LIQUID CRYSTAL DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**
CUSTOMER PART NUMBER	
PRODUCT NUMBER	**DBC-24032035-1A0**

Product Mgr	Design Eng
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Date: 22-Apr-10	Date: 22-Apr-10

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECN no.
1.0				First Issue	

1 MAIN FEATURES

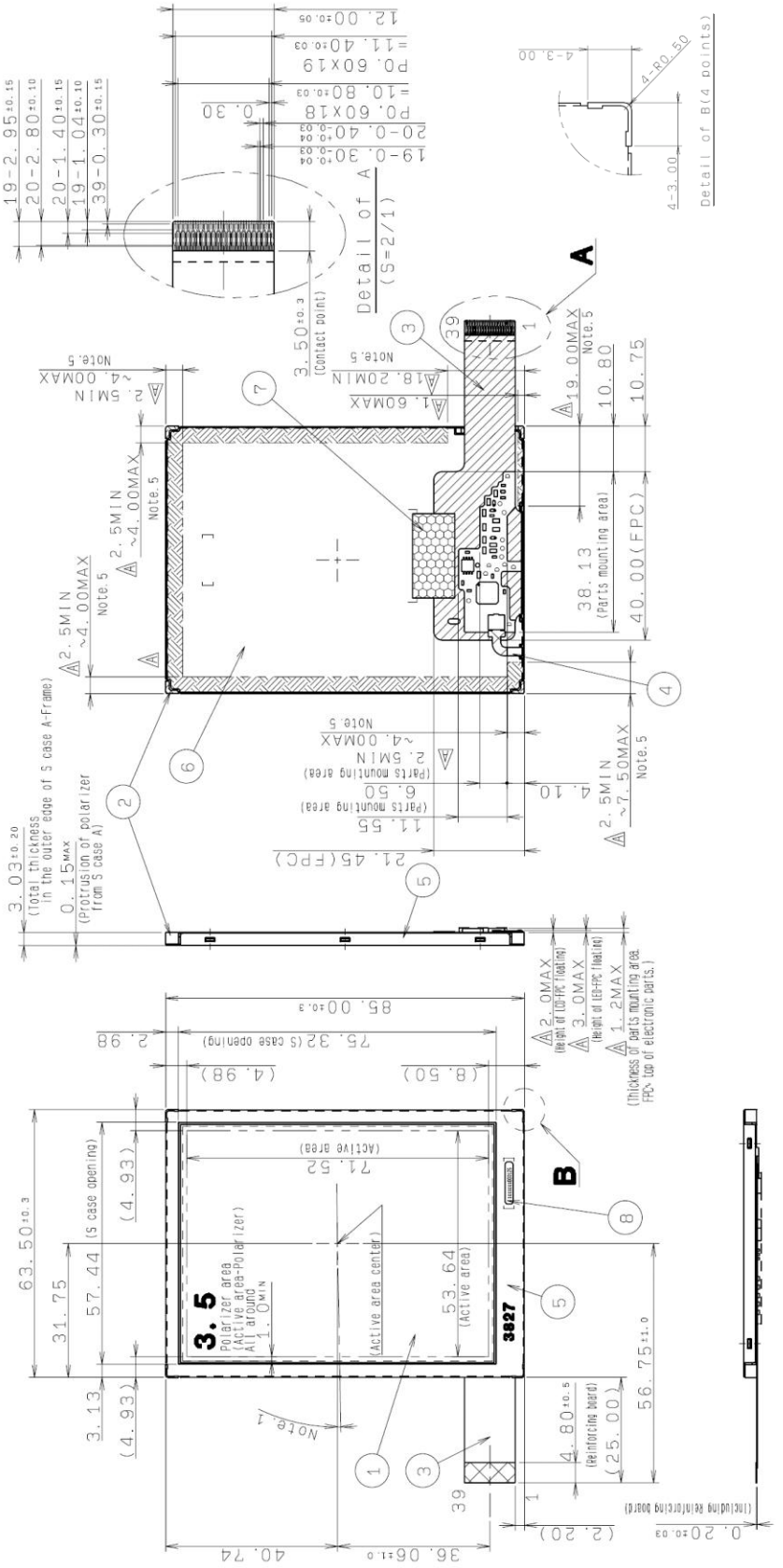
ITEM	CONTENTS
Screen Size	3.5” Diagonal
Display Format	240 x RGB x 320 Dots
N° of Colour	262k
Overall Dimensions	63.50 mm (H) x 85.00 mm (V) x 3.03 mm (D)
Active Area	53.64 mm (H) x 71.52 mm (V)
LCD Type	TFT
Mode	Sunlight Readable
Interface	6-bit RGB, parallel input
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	240 x RGB x 320	Dots
Overall Dimensions	63.50 (H) x 85.00 (V) x 3.03 (D)	mm
Bezel Opening Area	57.44 (H) x 75.32 (V)	mm
Active Area	53.64 (H) x 71.52 (V)	mm
Dot Pitch	74.5 (H) x RGB x 223.5 (V)	µm
Weight	33	g

2.2 MECHANICAL DRAWING



Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than ±40°.
Note 2. S label is affixed in the area shown in the drawing. The thickness of the S label will be added to that of S case's surface.
Note 3. Recommended FPC connectors. For LCD: HIROSE, part number: FH23-39S-0.3SHW(05)
Note 4. Protective film is affixed on front surface of the screen. Location tolerance of the protective film shall be ±1.5 mm to the polarising film.
Note 5. In case TFT-LCD monitor is fixed to the case of your product, it is recommended that monitor is fixed to area.
Note 6. Refer to "QUALITY ASSURANCE SPECIFICATION" about the appearance specification of a polarizer.

1. LCD
2. Frame
3. LCD-FPC
4. LED-FPC
5. S-Case A
6. S-Case C
7. Tape
8. S Label

2.3 SERIAL LABEL / PRINT

The label / print indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (4 or 5 characters), serial number (6 digits).

* Label / Print Contents

*	*	****(*)	******
a	b	c	d

where:

a The least significant digit of manufacturing year

b Manufacturing Month:
Jan-A, Feb-B, Mar-C, Apr-D, May-E, Jun-F, Jul-G, Aug-H, Sep-I, Oct-J, Nov-K, Dec-L

c Model code
35DQC →Made in Japan
35ENC →Made in Malaysia
35DRC →Made in China

d Serial number, like “000125”

Examples:

Made in Japan
0K35DQC000125
means "manufactured in November 2010, model 35DQC, serial number 000125"

Made in Malaysia
0K35ENC000125
means "manufactured in November 2010, model 35ENC, serial number 000125"

Made in China
0K35DRC000125
means "manufactured in November 2010, model 35DRC, serial number 000125"

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit	Applicable terminal
Supply Voltage	VDD	Ta=25˚C	-0.3	4.6	V	VDD
Input Voltage for Logic	VI		-0.3	VDD+0.3	V	CLK, VSYNC, HSYNC, DE, D[05;00], D[15;10], D[25;20], STBYB, RESETB, TEST1,TEST2

3.2 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable terminal
Supply Voltage	VDD		2.7	3.0	3.6	V	VDD
Input Voltage for Logic	VI		0	-	VDD	V	CLK, VSYNC, HSYNC, DE, D[05;00], D[15;10], D[25;20], STBYB, RESETB, TEST1,TEST2
Input Voltage for Logic	VIH		0.7xVDD	-	VDD	V	CLK, VSYNC, HSYNC, DE, STBYB, RESETB, D[05:00]; D[15:10], D[25:20] TEST1,TEST2
	VIL		0	-	0.3xVDD	V	
Current Consumption	IDD	fCLK=6.25MHz Colour bar display	-	6.8	13.6	mA	VDD

3.3 INTERFACE PIN ASSIGNMENT

3.3.1 LCM PIN ASSIGNMENT

Pin No.	Symbol	Function
1	VSS	Ground
2	VSS	Ground
3	VDD	Power supply
4	VDD	Power supply
5	VSS	Ground
6	RESETB	Reset signal. When RESETB is Lo, an internal reset is performed
7	HSYNC	Horizontal sync signal input. (Low active)
8	VSYNC	Vertical sync signal input. (Low active)
9	CLK	Clock signal for data latching and internal counter of the timing controller
10	VSS	Ground
11	D00	Display data (B) 00h: Black D00:LSB D05:MSB Driver has internal gamma conversion.
12	D01	
13	D02	
14	D03	
15	D04	
16	D05	
17	D10	Display data (G) 00h: Black D10:LSB D15:MSB Driver has internal gamma conversion.
18	D11	
19	D12	
20	D13	
21	D14	
22	D15	
23	D20	Display data (R) 00h: Black D20:LSB D25:MSB Driver has internal gamma conversion.
24	D21	
25	D22	
26	D23	
27	D24	
28	D25	
29	VSS	Ground
30	DE	Input data effective signal (it is effective for the period of “H”)
31	STBYB	Standby signal (Hi: Normal operation, Lo: Standby operation)
32	TEST1	Connect to Ground
33	NC	Open
34	NC	Open
35	NC	Open
36	NC	Open
37	TEST2	Connect to Ground.
38	BLH	LED drive power source (Anode side)
39	BLL	LED drive power source (Cathode side)

Recommended connector: Hirose Electric FH23 series [FH23-39S-0.3SHW(05)]
As FCB cable has gold plated terminals, gilt finish contact shoe connector is recommended.

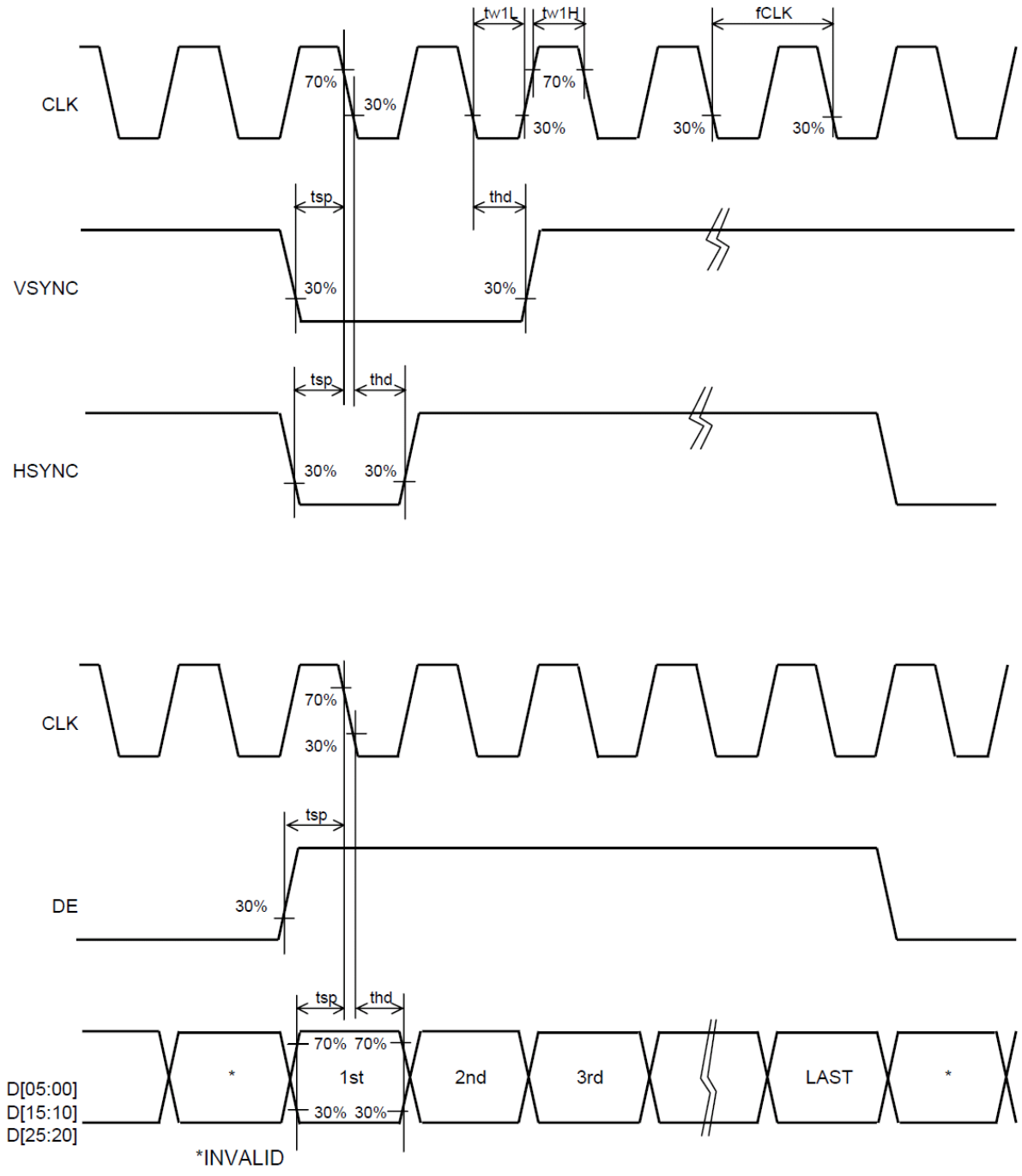
3.4 TIMING CHARACTERISTICS

3.4.1 AC Timing Characteristics

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
CLK frequency	fCLK		4.4	5.6	7.0	MHz	CLK
CLK Low period	tw1L	0.3xVDD or less	15	-	-	ns	
CLK High period	tw1H	0.7xVDD or more	15	-	-	ns	
Input Setup time	tsp		15	-	-	ns	CLK, VSYNC, HSYNC, DE, STBYBD[05:00], D[15:10], D[25:20]
Input Hold time	thd		15	-	-	ns	

3.4.2 AC Timing Diagrams

Switching Characteristics Wave Form



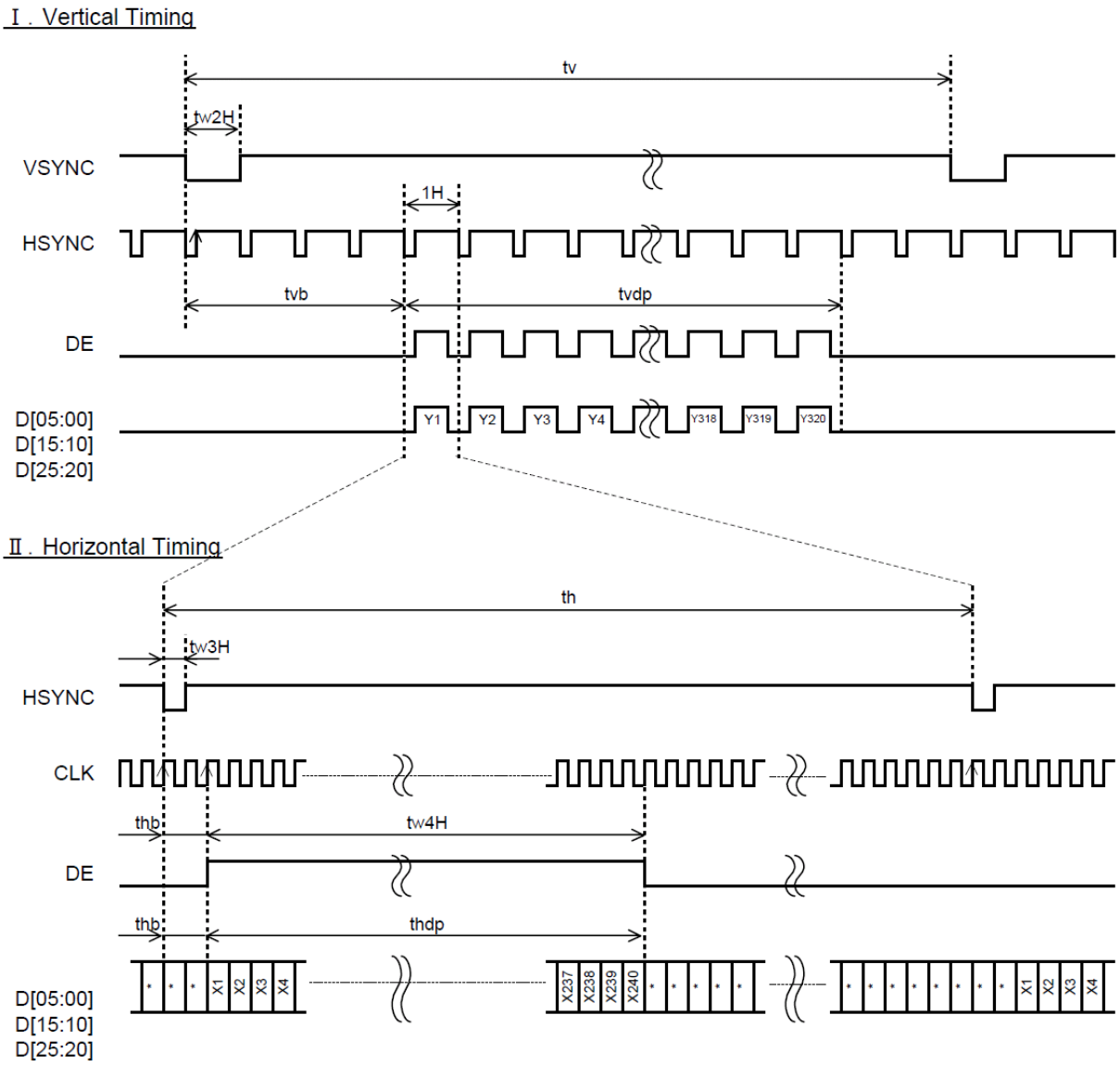
3.4.3 Input Timing Characteristics

Unless otherwise noted, Ta=25°C, VDD=3.3V, VSS=0V

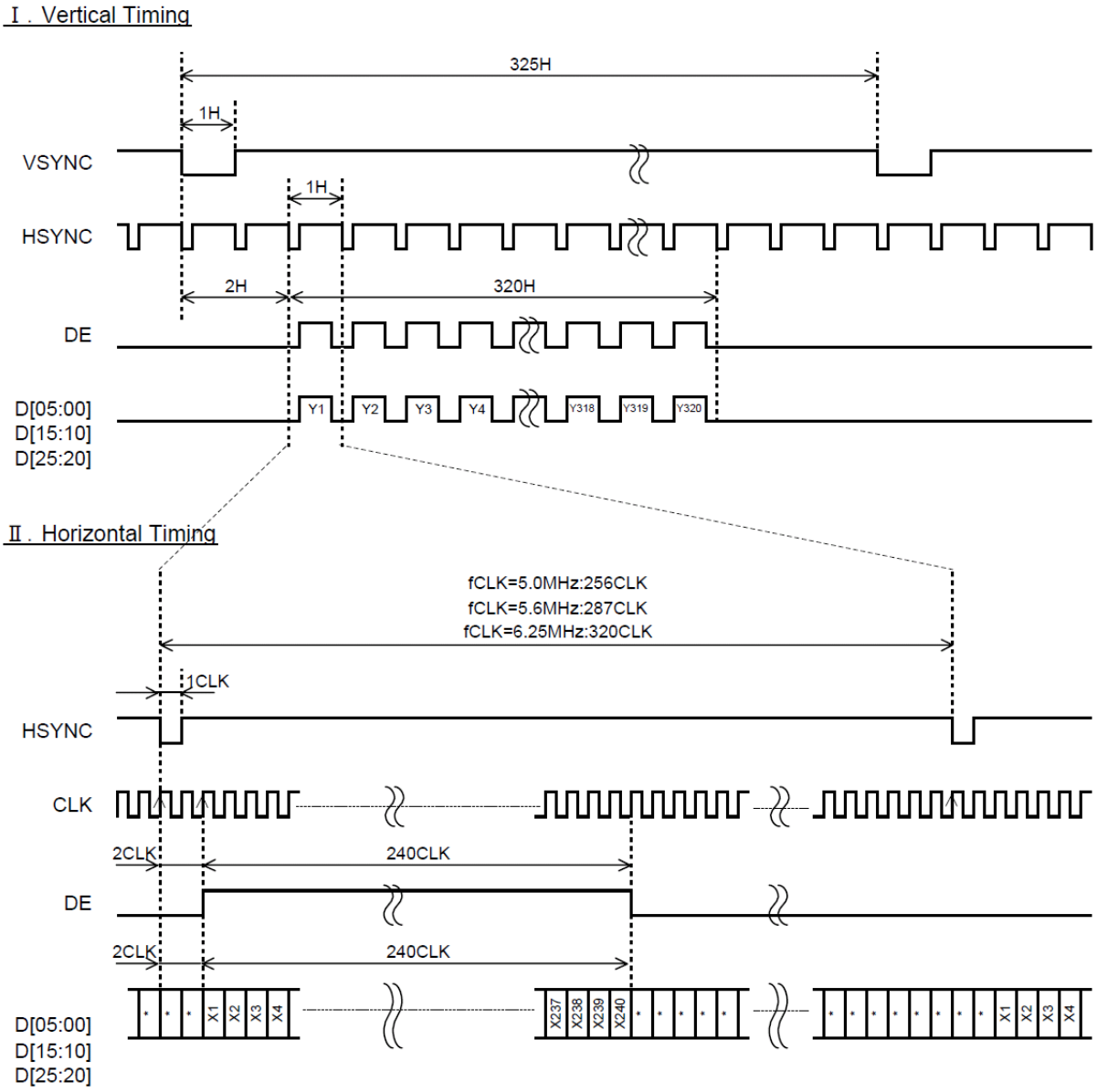
Item	Symbol	Rating			Unit	Applicable terminal
		MIN	TYP	MAX		
CLK frequency	fCLK	4.4	5.6	7.0	MHz	CLK
VSYNC frequency Note1	fVSYNC	54	60	66	Hz	VSYNC
VSYNC signal cycle time	tv	324	325	348	H	VSYNC, HSYNC
VSYNC pulse width	tw2H	1	-	-	H	
Vertical back porch	tvb	2	-	14	H	VSYNC, HSYNC, DE, D[05:00]; D[15:10], D[25,20]
Vertical display period	tvdp	-	320	-	H	VSYNC, HSYNC, DE, D[05:00], D[15:10], D[25:20]
HSYNC frequency	fHSYNC	-	19.5	-	KHz	HSYNC
HSYNC signal cycle time	th	-	287	402	CLK	HSYNC, CLK
HSYNC pulse width	tw3H	1	-	-	CLK	
Horizontal back porch	thb	2	-	14	CLK	HSYNC, DE, CLK, D[05:00], D[15:10], D[25:20]
DE pulse width	tw4H	-	240	-	CLK	DE, CLK
Horizontal display period	thdp	-	240	-	CLK	DE, D[05:00], D[15:10], D[25:20], CLK

Note 1:The characteristic of this item is recommended as standard.

3.4.4 Driving Timing Chart

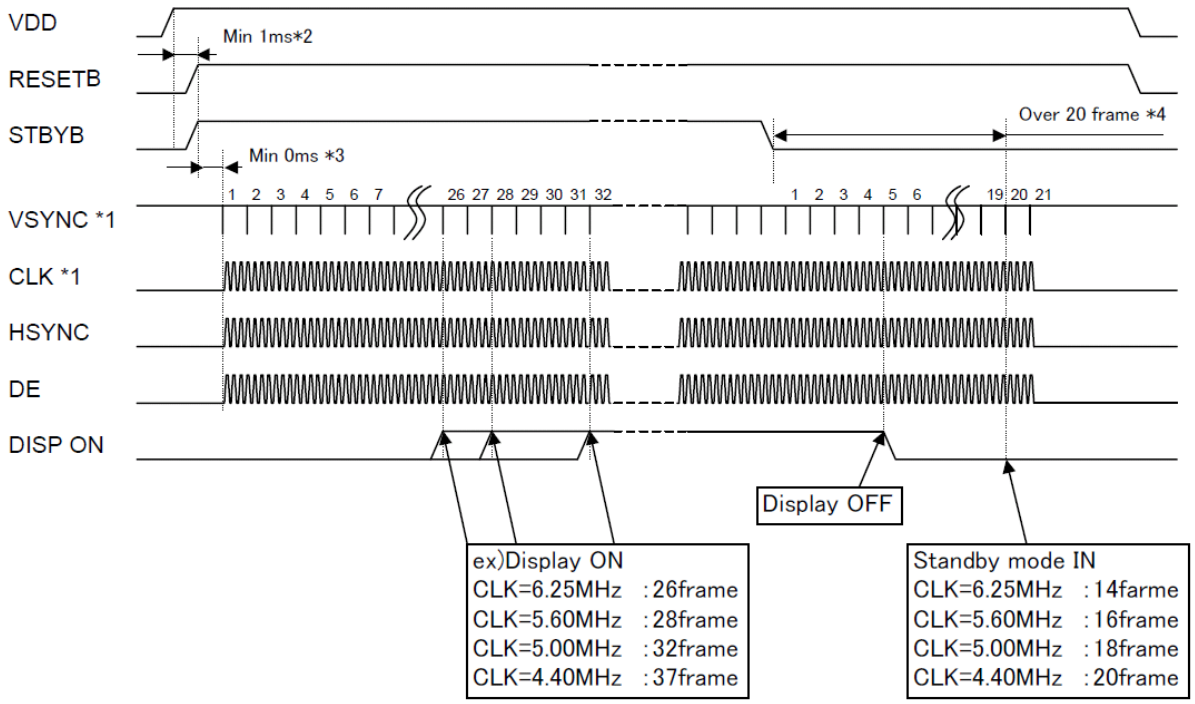


3.4.5 Example of Input Timing Chart (fCLK= 5.0MHz, 5.6MHz, 6.25MHz)



3.5 POWER SEQUENCE

3.5.1 Power ON/OFF Sequence



*1 DOTCLK is used for Gate array CLK on FPC
VSYNC is used for Gate array's inside counter.
It becomes the operation after CLK(DOTCLK),VSYNC input.

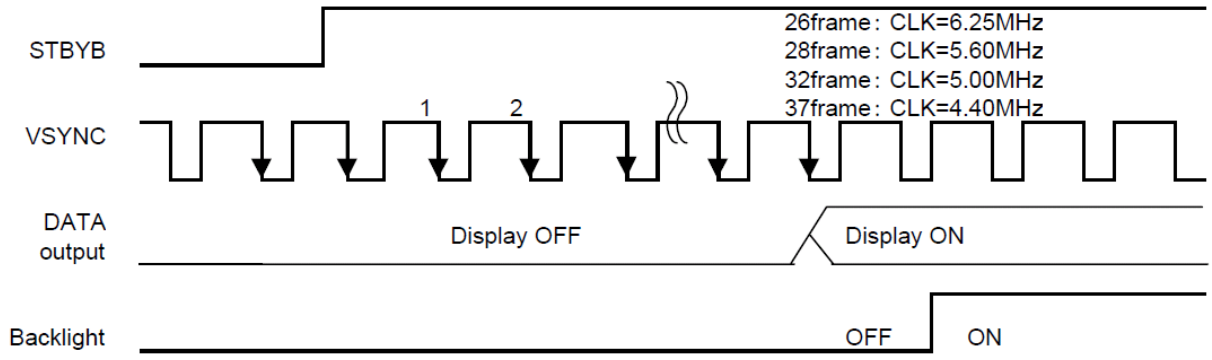
*2 After the power supply. Please execute RESETB (refer to reset sequence)

*3 There is no regulation at time until each signal is supplied from RESETB"H"
But meanwhile, It is necessary to fix each signal to "H"or"L".

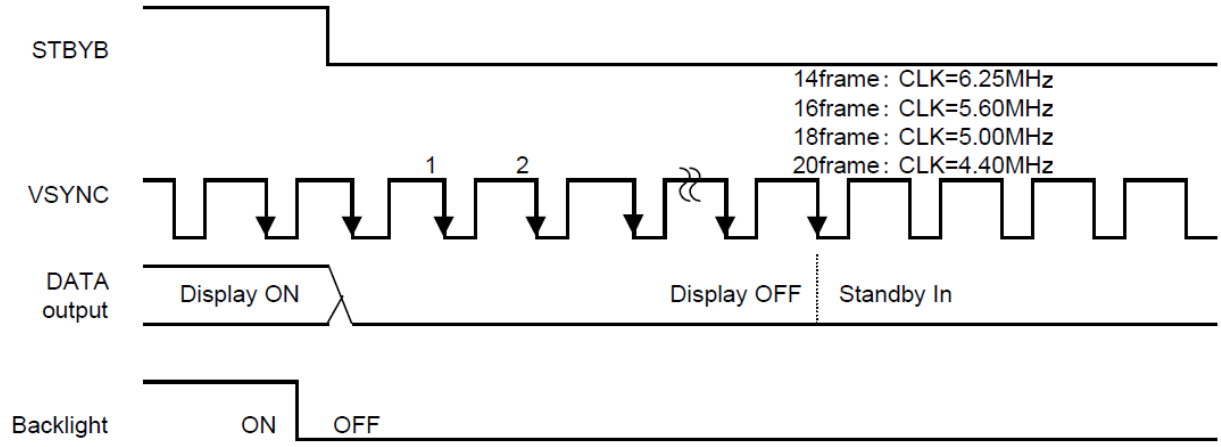
*4 It is necessary to supply VSYNC and CLK(DOTCLK) for 20 frames or less from STBYB "L" to turning off the power supply without leaving the afterimage.

3.5.2 Display ON/OFF sequence

It explains the display sequence when display ON/OFF by the STBYB signal.
The following time will be needed according to the CLK cycle by the time the displays begun from the standby release.

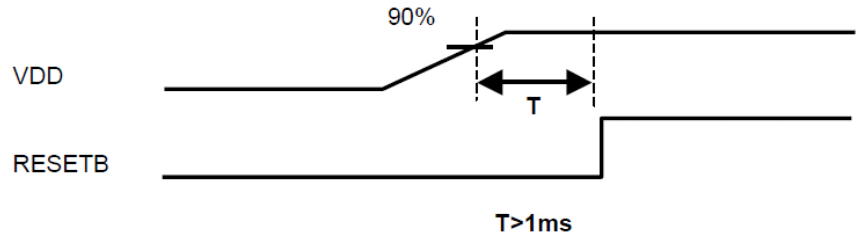


The following time will be needed according to the CLK cycle by the time the standby sequence is ended from the standby setting. Meanwhile, DOTCLK and the VSYNC signal should keep being supplied. When DOTCLK and the VSYNC signal are stopped or the power supply is turned off to a regulated frame or less, the afterimage might remain.



3.5.3 Reset sequence

There is a limitation between the power supply turning on and the RESETB input.
Please defend the following conditions.



T>1ms

4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Measuring instruments: CS1000（KONICA MINOLTA), LCD7000 (OTSUKA ELECTRONICS)
EZcontrast160D（ELDIM)
Driving condition: VDD = 3.0V, VSS = 0V
Optimized Vcom/c
VLCD=｜Vsigpp±Vcompp｜/2
Backlight: IL=10mA
Measured temperature: Ta ＝ 25° C

Ta = 25 °C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Note
Response Time	Rise Time	TON	VLCD=0.5V→4.8V	-	-	40	ms	1	*
	Fall Time	TOFF	VLCD=4.8V→0.5V	-	-	60	ms		
Contrast Ratio	Backlight ON	CR	VLCD= 0.5V/4.8V	240	400	-		2	
	Backlight OFF			-	6.5	-			
Viewing Angle	Left	θL	VLCD= 0.5V/4.8V CR ≥ 10	80	-	-	deg	3	*
	Right	θR		80	-	-	deg		
	Up	φU		80	-	-	deg		
	Down	φD		80	-	-	deg		
V-T Threshold Voltage		V90		1.2	1.5	1.8	V	4	*
		V50		1.7	2.0	2.3	V		
		V10		2.4	2.7	3.0	V		
White V-T Curve				Refer to Fig. 3 : White V-T Curve					Reference
White Chromaticity		x	VLCD= 0.5V	Fig. 4: White Chromaticity Range				5	
		y							
Burn-in				No noticeable burn-in image should be observed after 2hours of window pattern display.				6	
Centre Brightness			VLCD= 0.5V	175	250	-	cd/m²	7	
Brightness Distribution			VLCD= 0.5V	70	-	-	%	8	

* Measured in the form of LCD module

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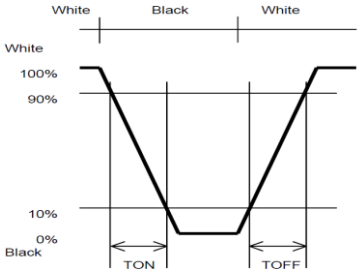
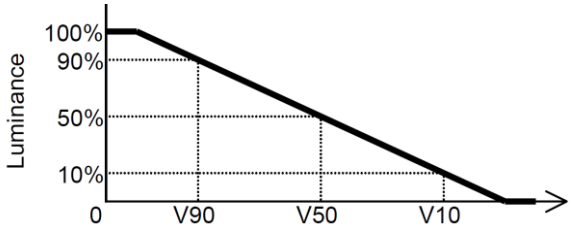
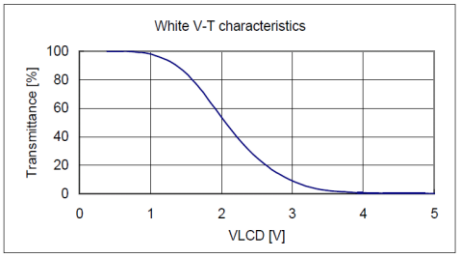
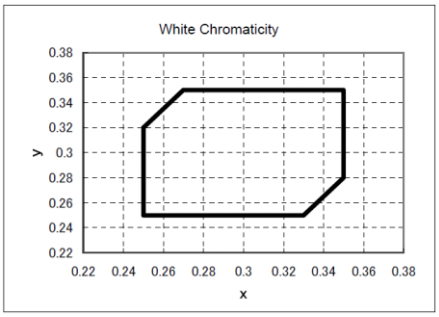
4.1.1 Test Method

Note	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 	LCD7000	Black display VLCD=4.8V White display VLCD=0.5V TON Rise Time TOFF Fall Time
2	Contrast ratio	Measure maximum luminance Y1 (VLCD=0.5V) and minimum luminance Y2 (VLCD=4.8V) at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2 Diameter of measuring point: 8mm Ø	CS1000 LCD7000	Backlight ON Backlight OFF
3	Viewing angle Horizontal θ Vertical Ø	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10	EZcontrast160D	
4	V-T Threshold Value	Change VLCD by 0.1V step and plot the points where the luminance is 90% as V90, 50% as V50 and 10% as V10 of maximum luminance. 	LCD7000	
5	White chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system at VLCD=0.5V Colour matching faction: 2° view	CS1000	
6	Burn-in	Visually check burn-in image on the screen after 2 hours of “window display” (VLCD=0.5V/4.8V).		At optimized Vcom/C
7	Centre brightness	Measure the brightness at the centre of the screen	CS1000	
8	Brightness distribution	(Brightness distribution)= 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points	CS1000	





【White Chromaticity Range】

x	y
0.25	0.32
0.25	0.25
0.33	0.25
0.35	0.28
0.35	0.35
0.27	0.35

5 BACKLIGHT SPECIFICATION

5.1 LED DRIVING CONDITIONS

Item	Symbol	Condition	Rating			Unit	Applicable Terminal
			Min	Typ	Max		
Forward Current	IL25	Ta=25 °C	-	10	35	mA	BLH-BLL
	IL70	Ta= 70°C	-		15	mA	
Forward Voltage	VL	Ta= 25°C, IL= 10mA	-	18.0	19.7	V	
Estimated Life of LED	LL	Ta= 25°C, IL= 10mA Note	-	(50,000)	-	hr	

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
  The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

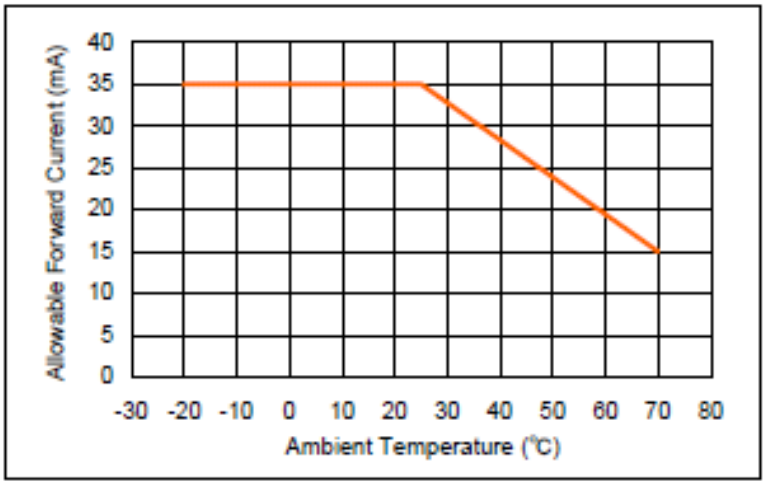
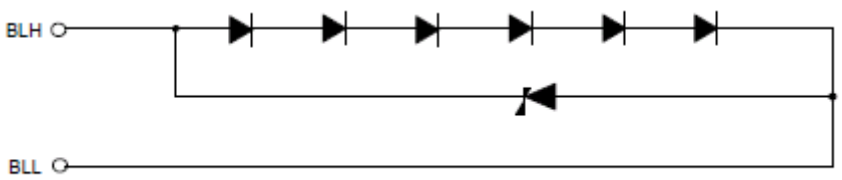


Fig. 2: Allowable Forward Current

5.2 LED CIRCUIT



6 QUALITY ASSURANCE SPECIFICATION

6.1 DEFECTIVE DISPLAY AND SCREEN QUALITY

Observed TFT-LCD monitor from front during operation with the following conditions

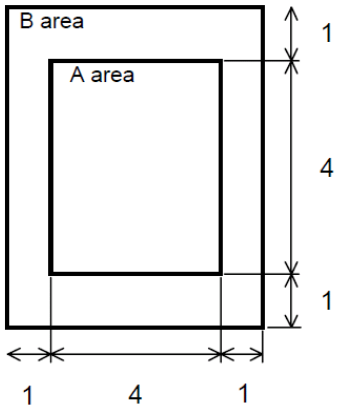
Driving signal	Raster Pattern (RGB in monochrome, white black)
Signal condition	VLCD: 0.5V, 2.6 V, 4.8V (3 Steps)
Observation Distance	30cm
Illuminance	200 to 350 lx
Backlight	IL= 10mA

Defect item		Defect content		Criteria
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots		Not exists
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at VLCD=4.8V Low bright dot: Visible through 5% ND filter at VLCD=4.8V Dark dot: Appear dark through white display at VLCD=2.6V		Refer to Table 1
Screen Quality	Dirt	Point-like uneven brightness (white stain, black stain etc)		Invisible through 1% ND filter
	Foreign particle	Point-like	0.25mm< ϕ	N=0
			0.20< ϕ ≦0.25mm	N≦2
			ϕ ≦0.20mm	Ignored
		Liner	3.0mm<length and 0.08mm<width	N=0
			length≦3.0mm or width ≦0.08mm	Ignored
	Others			Use boundary sample for judgment when necessary

ϕ (mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more
B	2	4	4	6	Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
Total	2	4	4	7	



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

6.2 SCREEN AND OTHER APPEARANCE

Testing conditions
Illuminance 1200~2000 lx
Observation distance 30cm

Item		Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only (Refer to the section 3.2 "Outward Form")
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	

6.3 DEALING WITH CUSTOMER COMPLAINTS

6.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.3.2 Handling of non-conforming displays

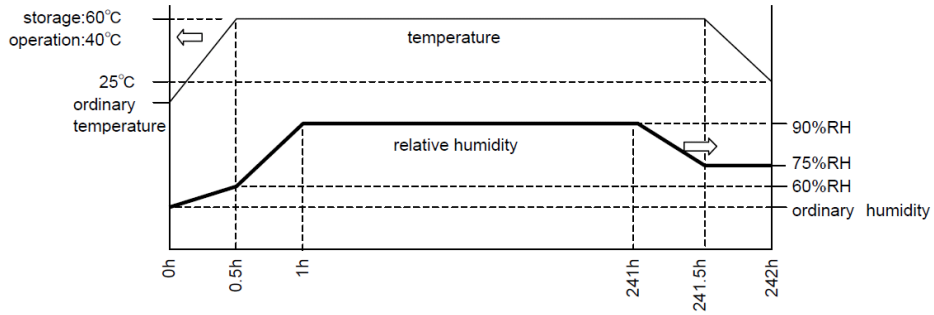
If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7 RELIABILITY SPECIFICATION

7.1 RELIABILITY TESTS

Test Item		Test Condition	Number of failures/ number of examinations
Durability Test	High Temperature Storage	Ta= 80˚C 240h	0/3
	Low Temperature Storage	Ta=-30˚C 240h	0/3
	High Temperature & High Humidity Storage	Ta= 60°C, RH= 90% Non condensing 240h	0/3
	High Temperature Operation	Tp= 70°C 240h	0/3
	Low Temperature Operation	Tp= -20°C 240h	0/3
	High Temperature & Humidity Operation	Tp= 40°C RH= 90% 240h Non condensing	0/3
	Thermal Shock Storage	-30←→ 80°C (30 min/ 30min) 100cycles	0/3
Mechanical Environmental Test	Electrostatic Discharge Test (non operation)	Confirms to EIAJ ED-4701/300 C= 200 pF, R= 0 Ω, V= ±200V Each 3 times of discharge on and power supply and other terminals.	0/3
	Surface Discharge Test (non operation)	C= 250 pF, R= 100 Ω, V=± 12kV Each 5 times of discharge in both polarities on the centre of screen with the case grounded.	0/3
	Vibration test	Total amplitude 1.5 mm, f= 10~55 Hz, X,Y,Z directions for each 2 hours.	0/3
	Impact test	Use original jig and make an impact with peak acceleration of 1000 m/s²for 6 ms with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-1995	0/3
Packing Test	Packing Vibration-Proof Test	Acceleration of 19.6 m/s ² with frequency of 10 → 55→ 10 Hz, X, Y, Z direction for each 30 minutes.	0/1 Packing
	Packing Drop Test	Drop from 75 cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	0/1 Packing

Note: Ta=ambient temperature Tp= Panel temperature



Reliability Criteria: measure following parameters after leaving the TFT at 25°C for 2 hours or more.

Item	Standard	Remark
Display quality	No visible abnormalities shall be seen	As per Quality Assurance Specification
Contrast ratio	40 or more	Backlight ON

8 HANDLING PRECAUTIONS

Safety
If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.
If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS.
Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).