LIQUID CRYSTAL DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**
CUSTOMER PART NUMBER	
PRODUCT NUMBER	**DBC-64048057-2B0**

Product Mgr	Design Eng
Bruno Recaldini	**Luo Luo**
Date: 02-Dec-11	Date: 02-Dec-11

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECN no.
2.0				First Issue	

1 MAIN FEATURES

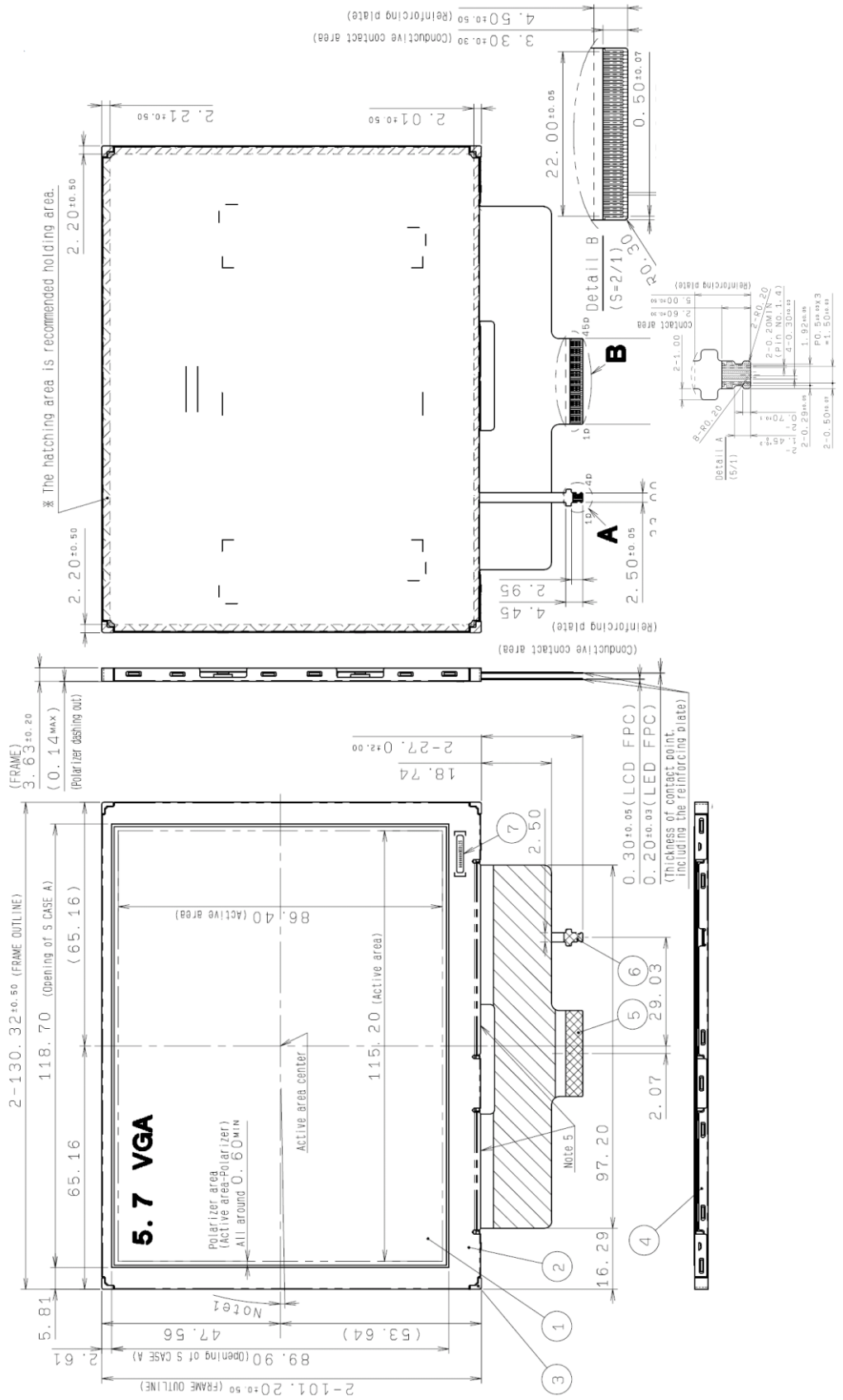
ITEM	CONTENTS
Screen Size	5.7” Diagonal
Display Format	640 x RGB x 480 Dots
N° of Colour	262k
Overall Dimensions	130.32 mm (H) x 101.20 mm (V) x 3.63 mm (D)
Active Area	115.20 mm (H) x 86.40 mm (V)
LCD Type	TFT
Mode	Sunlight Readable
Interface	6-bit RGB, parallel input
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	640 x RGB x 480	Dots
Overall Dimensions	130.32 (H) x 101.20 (V) x 3.63 (D)	mm
Bezel Opening Area	118.70 (H) x 89.90 (V)	mm
Active Area	115.20 (H) x 86.40 (V)	mm
Dot Pitch	60.0 (H) x RGB x 180.0 (V)	µm
Weight	85	g

2.2 MECHANICAL DRAWING



1. LCD
2. S case A
3. Frame
4. S Case C
5. LCD FPC
6. LED FPC
7. S label

Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than ±50°.
Note 2. S label is affixed in the area shown in the drawing. The thickness of S label will be added to that of S case's surface.
Note 3. Protective film is affixed on front surface of the screen. Location tolerance of the protective film shall be ±1.5 mm to the polarising film
Note 4. Exercise care not to apply any force to the cable holder of the S case A.
Note 5. Refer to "QUALITY ASSURANCE SPECIFICATION" about the appearance specification of the polariser.
Note 6. Recommended FPC connector:
For LCD: KYOCERA ELCO 6240 series, part number 04 6240 045 023 846+ (lower contact)
For LED: KYOCERA ELCO 6277 series, part number 04 6277 004 001 883+ (lower contact)

2.3 SERIAL LABEL / PRINT

The label / print indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (4 or 5 characters), serial number (6 digits).

* Label / Print Contents

*	*	****(*)	******
a	b	c	d

where:

a The least significant digit of manufacturing year

b Manufacturing Month:
Jan-A, Feb-B, Mar-C, Apr-D, May-E, Jun-F, Jul-G, Aug-H, Sep-I, Oct-J, Nov-K, Dec-L

c Model code
57CKC →Made in Japan
57CLC →Made in Malaysia
57CMC →Made in China

d Serial number, like “000125”

Examples:

Made in Japan
0K57CKC000125
means "manufactured in November 2010, model 57CKC, serial number 000125"

Made in Malaysia
0K57CLC000125
means "manufactured in November 2010, model 57CLC, serial number 000125"

Made in China
0K57CMC000125
means "manufactured in November 2010, model 57CMC, serial number 000125"

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit	Applicable terminal
Supply Voltage for Logic	VDD	Ta=25˚C Note 1	-0.3	7.0	V	VDD
Supply Voltage for Analogue 1	AVVD		-0.3	13.5	V	AVDD
Supply Voltage for Analogue 2	VGH		-0.3	42.0	V	VGH
Supply Voltage for Analogue 3	VGL		VGH-42.0	0.3	V	VGL
Supply Voltage for Analogue 4 Note2	Vy		-0.3	AVDD-0.1	V	V1, V5, V6, V10
Input Voltage for Logic	VI		-0.3	VDD+0.3	V	CLK, VSYNC, HSYNC, DE, D[05;00], D[15;10], D[25;20], RL, UD, DISP, TEST1~6, POCB
Common electrode voltage	VCOM		-0.3	10.0	V	VCOM

Note 1: please refer to the “Power ON/OFF Sequence” section
Note 2: AVDD>V1>V5>V6>V10>VSS

3.2 ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, Ta=25°C, VDD=3.3V, VSS=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable terminal
Supply Voltage for logic	VDD		3.0	3.3	3.6	V	VDD
Supply Voltage for Analogue 1	AVDD		11.0	12.0	13.0	V	AVDD
Supply Voltage for Analogue 2	VGH		20.0	21.0	22.0	V	VGH
Supply Voltage for Analogue 3	VGL		-8.0	-7.0	-6.0	V	VGL
Common electrode voltage Note1	VCOM		4.2	4.7	5.2	V	VCOM
Contrast range	V1		10.3	10.6	10.9	V	V1
	V5		6.9	7.2	7.5	V	V5
	V6		5.2	5.5	5.8	V	V6
	V10		0.7	0.8	0.9	V	V10
Input voltage for logic	VI		0	-	VDD	V	CLK, VSYNC, HSYNC, DE, D[05;00], D[15;10], D[25;20], RL, UD, DISP, POCB

Note 1: this range indicates the most probable range for the optimal setting for VCOM.
It does not mean that the optimal setting for VCOM for all TFT will be in this range.
VCOM should be optimised by viewing / using the display.

(Unless otherwise noted, Ta=25°C, VDD=3.3V, VSS=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable terminal
Input voltage for logic	VIH		0.7xVDD	-	VDD	V	CLK, VSYNC, HSYNC, DE, D[05;00], D[15;10], D[25;20], RL, UD, DISP, POCB
	VIL		0	-	0.3xVDD	V	
Pull up resistor value	Rpu		300	450	600	kΩ	DISP, POCB
Pull down resistor value	Rpd		300	450	600	kΩ	DE, D[05;00], D[15;10], D[25;20], TEST1~6
Current consumption	IDD	fCLK=25MHz Colour bar display VDD=3.3V AVDD=12.0V VGH=21.0V VGL=-7.0V	-	7.0	14.0	mA	VDD
	IAVDD		-	14.0	28.0	mA	AVDD
	IGH		-	120	240	µA	VGH
	IGL		-240	-120	-	µA	VGL

3.3 INTERFACE PIN ASSIGNMENT

3.3.1 LCM Pin Assignment

Pin No.	Symbol	Function
1	VSS	Ground
2	VGL	Negative voltage for gate driver
3	VDD	Power supply for logic circuit
4	VGH	Positive voltage for gate driver
5	AVDD	Power supply for analogue circuit
6	V10	Source driver output level voltage (negative case)
7	V6	Source driver output level voltage (negative case)
8	V5	Source driver output level voltage (positive case)
9	V1	Source driver output level voltage (positive case)
10	POCB	Power on clear (active Low)
11	DISP	Display on/off control signal (Lo: display off, HI: display on)
12	RL	Horizontally Flipped (right/left) Signal (Lo: horizontally flipped display, Hi: Normal display)
13	UD	Vertically Flipped (up/down) Signal (Lo: Normal display , Hi: vertically flipped display)
14	VSS	Ground
15	VDD	Power supply for logic circuit
16	DE	Input data effective signal (it is effective for the period of “Hi”)
17	HSYNC	Horizontal sync signal (Low active)
18	VSYNC	Vertical sync signal (Low active)
19	CLK	Clock signal (latching data on the rising edge)
20	TEST5	Connect to Ground
21	TEST6	Connect to Ground.
22	D00	Display data (R) 00h: Black D00:LSB D05:MSB Driver has internal gamma conversion.
23	D01	
24	D02	
25	D03	
26	D04	
27	D05	
28	TEST3	Connect to Ground
29	TEST4	Connect to Ground.
30	D10	Display data (G) 00h: Black D10:LSB D15:MSB Driver has internal gamma conversion.
31	D11	
32	D12	
33	D13	
34	D14	
35	D15	
36	TEST1	Connect to Ground
37	TEST2	Connect to Ground.

Pin No.	Symbol	Function
38	D20	Display data (B) 00h: Black D20:LSB D25:MSB Driver has internal gamma conversion.
39	D21	
40	D22	
41	D23	
42	D24	
43	D25	
44	VCOM	Input signal for common electrode
45	VSS	Ground

Recommended connector: KYOCERA ELCO 6240 series [04 6240 045 023 846+]
Please refer to the section 2.2 for pin terminal order.
Since FPC cable has gold plated terminals, gilt finish contact shoe connector is recommended.

3.3.2 LED Backlight Pin Assignment

Pin No.	Symbol	Function
1	BLH1	Backlight 1 (Anode)
2	BLH2	Backlight 2 (Anode)
3	BLL2	Backlight 2 (Cathode)
4	BLL1	Backlight 1 (Cathode)

Recommended connector: KYOCERA ELCO 6277 series [04 6277 004 001 883+]
Please refer to the section 2.2 for pin terminal order.
Since FPC cable has gold plated terminals, gilt finish contact shoe connector is recommended.

3.4 TIMING CHARACTERISTICS

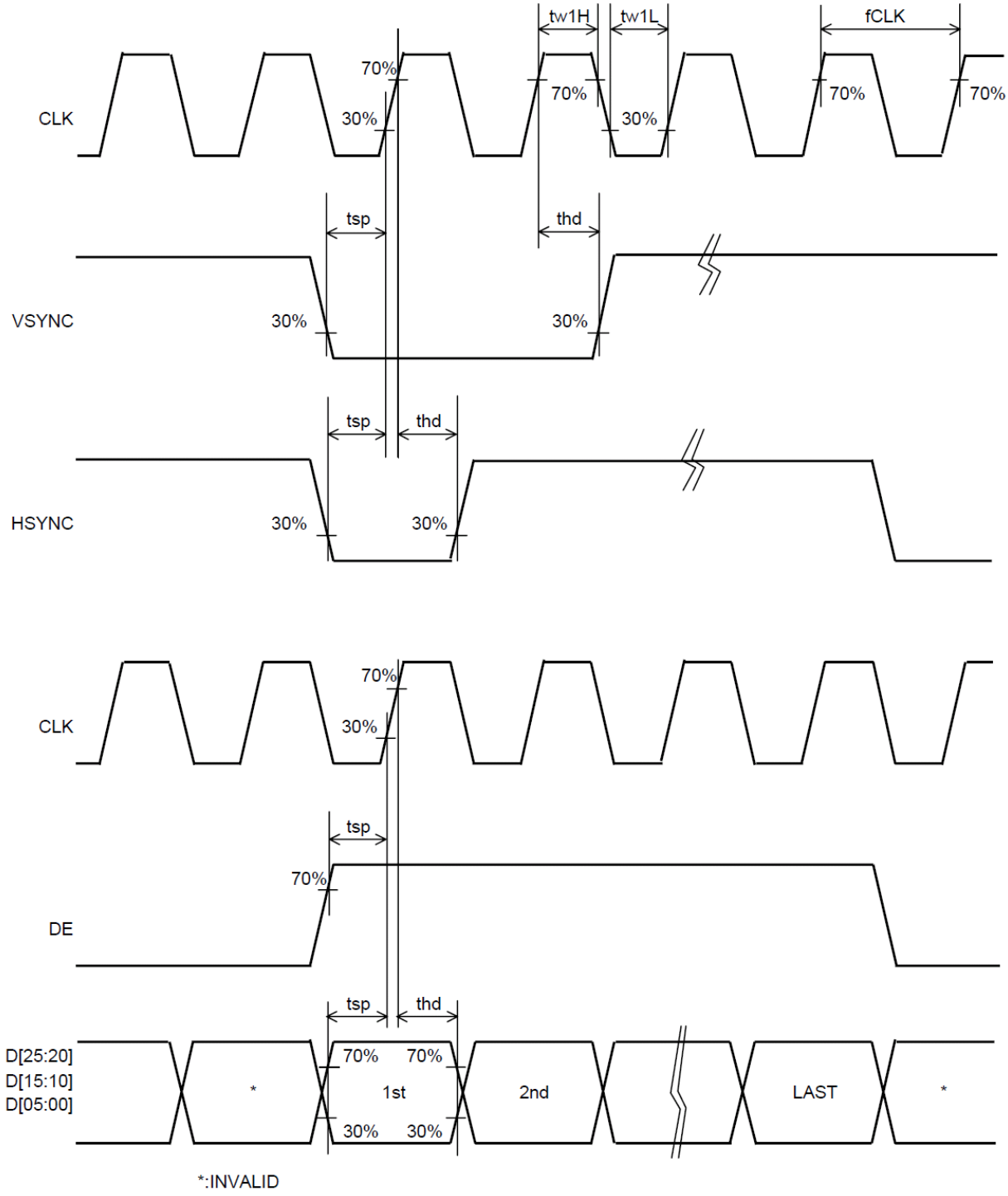
3.4.1 AC Timing Characteristics

(Unless otherwise noted, Ta=25°C, VDD=3.3V, VSS=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
CLK frequency	fCLK			25	27	MHz	CLK
CLK Low period	tw1L	0.3xVDD or less	14.8	-	-	ns	
CLK High period	tw1H	0.7xVDD or more	14.8	-	-	ns	
Setup time	tsp		10	-	-	ns	CLK, VSYNC, HSYNC, DE, D[05:00], D[15:10], D[25:20]
Hold time	thd		10	-	-	ns	

3.4.2 AC Timing Diagrams

Switching Waveform Characteristics



3.4.3 Input Timing Characteristics

Unless otherwise noted, Ta=25°C, VDD=3.3V, VSS=0V

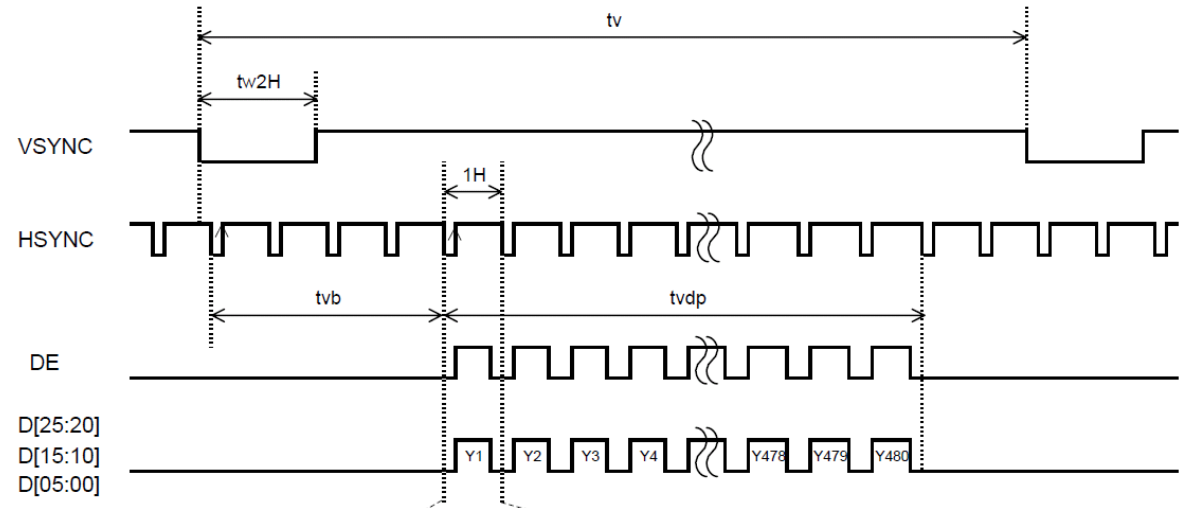
Item	Symbol	Rating			Unit	Applicable terminal
		MIN	TYP	MAX		
CLK frequency	fCLK	-	25	27	MHz	CLK
VSYNC frequency Note1	fVSYNC	54	60	66	Hz	VSYNC
VSYNC signal cycle time	tv	-	525	-	H	VSYNC, HSYNC
VSYNC pulse width	tw2H	1	3	5	H	
Vertical back porch	tvb	-	35	-	H	VSYNC, HSYNC, DE, D[05:00]; D[15:10], D[25,20]
Vertical display period	tvdp	-	480	-	H	
HSYNC signal cycle time	th	-	800	-	CLK	HSYNC, CLK
HSYNC pulse width	tw3H	5	30	-	CLK	
Horizontal back porch	thb	112	-	144 Note 2	CLK	HSYNC, DE, CLK, D[05:00], D[15:10], D[25:20]
Horizontal display period	thdp	-	640	-	CLK	
DE pulse width	tw4H	-	640	-	CLK	DE, CLK

Note 1: The characteristic of this item is recommended as standard. Please use it after it confirms it enough like the display fineness etc. When it comes off from this characteristic and it is used.

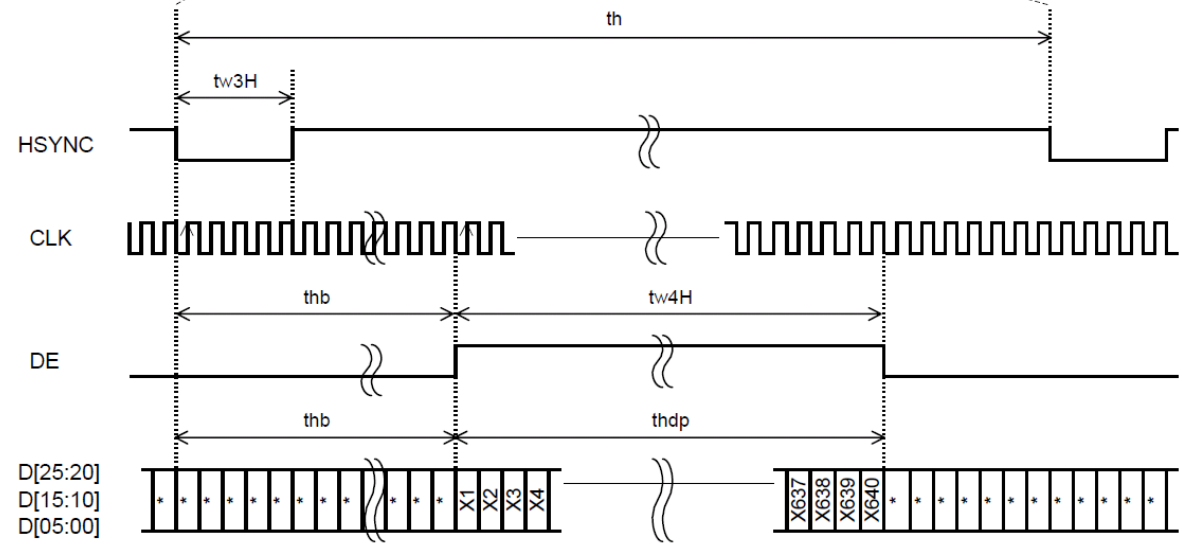
Note2: When "DE" keeps "Lo" for 144CLK or longer, start capturing data automatically from 144CLK.

3.4.4 Driving Timing Chart

-Vertical Timing

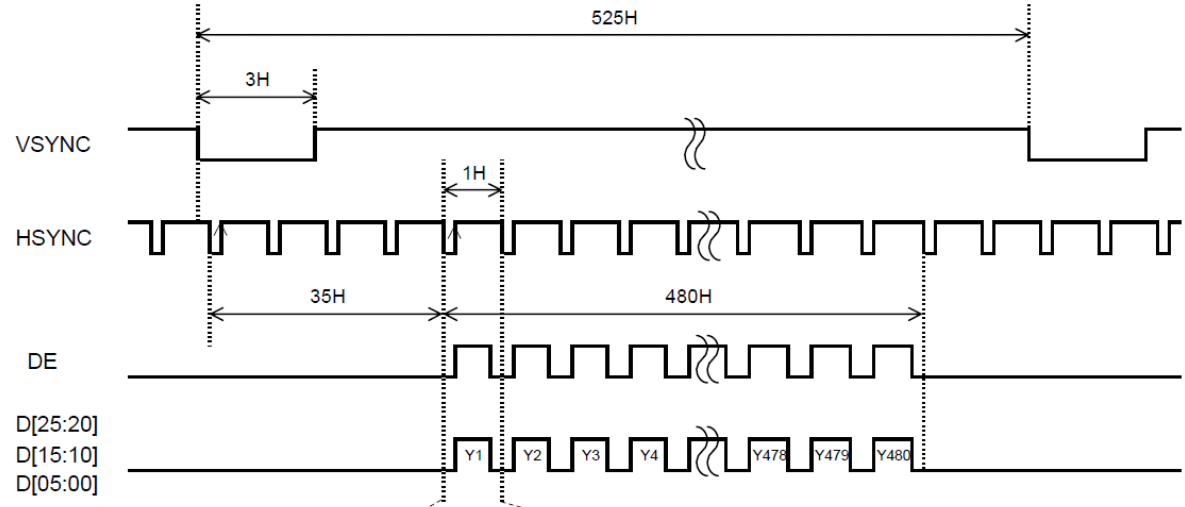


-Horizontal Timing

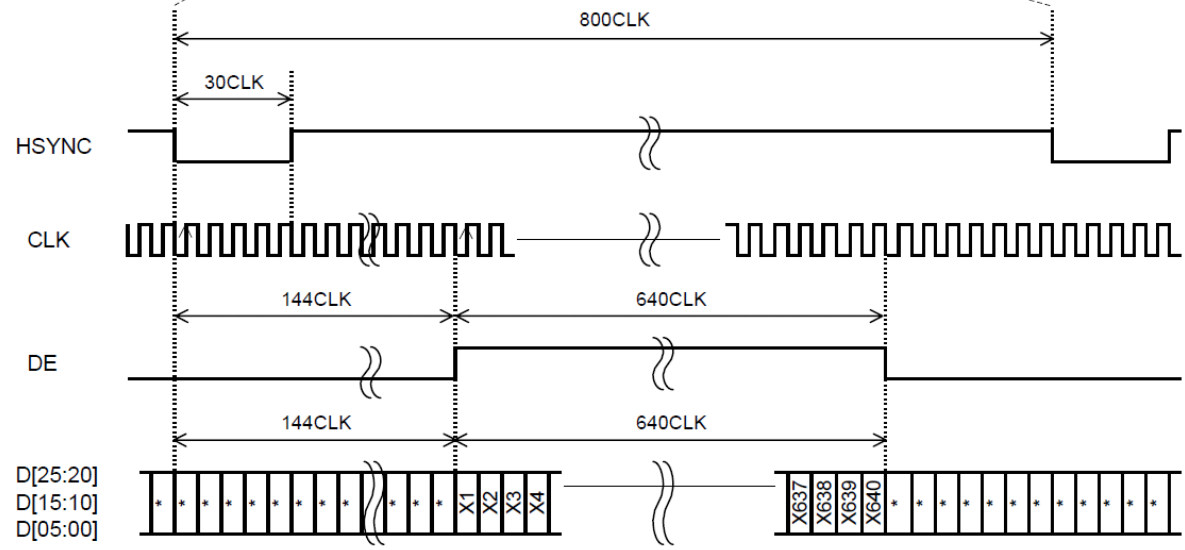


3.4.5 Example of Driving Timing Chart (fCLK= 25MHz)

-Vertical Timing



-Horizontal Timing



3.5 POWER SEQUENCE

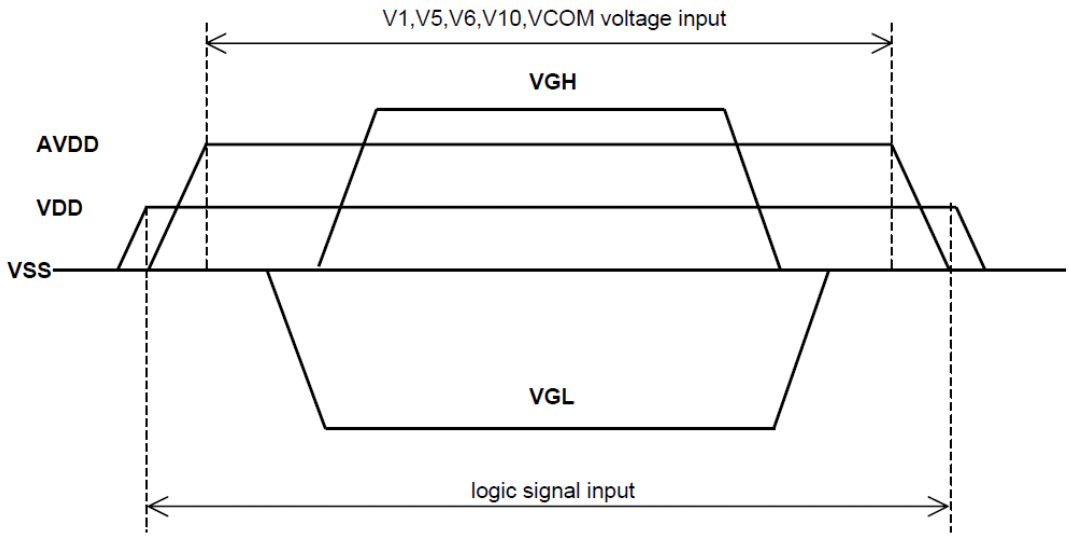
3.5.1 Display ON/OFF Sequence

The sequence of the Power On/Off and the signal input must defend the following conditions.

- Please input the logic signal after turning on VDD.
- Please input AVDD after turning on VDD or at the same time.
- Please input V1, V5, V6, V10 and VCOM voltage after turning on AVDD.
- Please input VGL after turning on VDD.
- Please input VGH after turning on VGL.

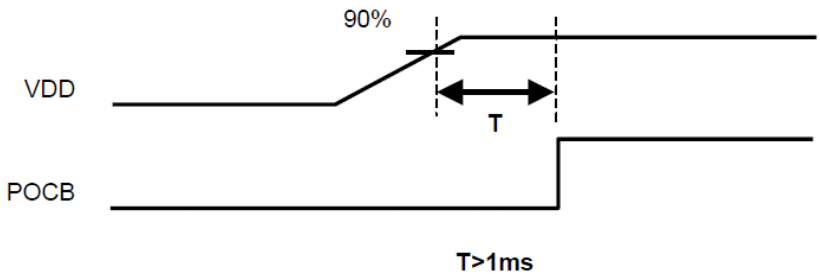
Power Off sequence is assumed to be opposite of the above mentioned sequence.

Power On/Off recommended sequence is shown in the figure below.



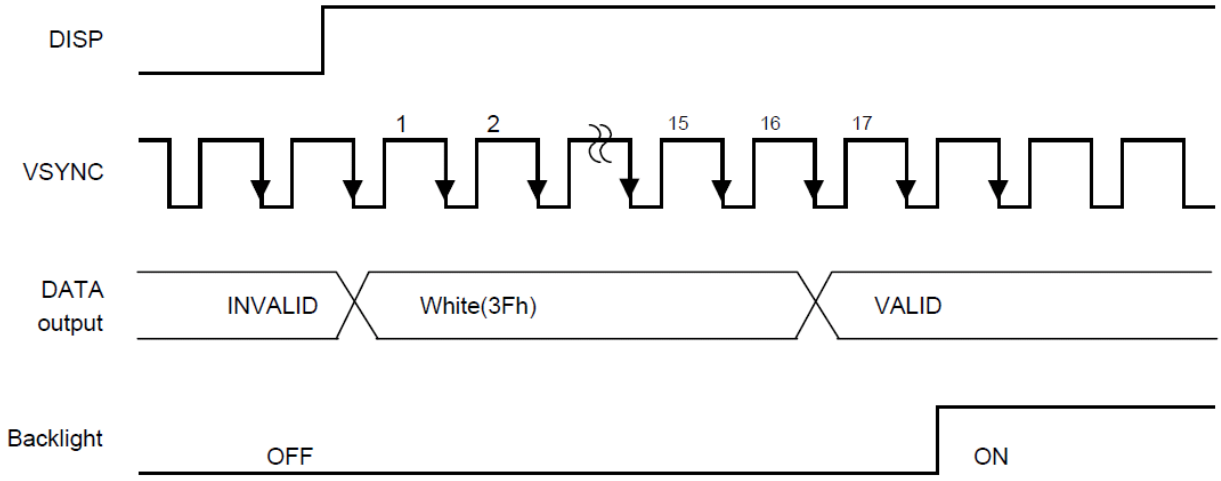
3.5.2 Power On Clear

There is a limitation between Power On and POCB (power on clear).
Please defend the following conditions.

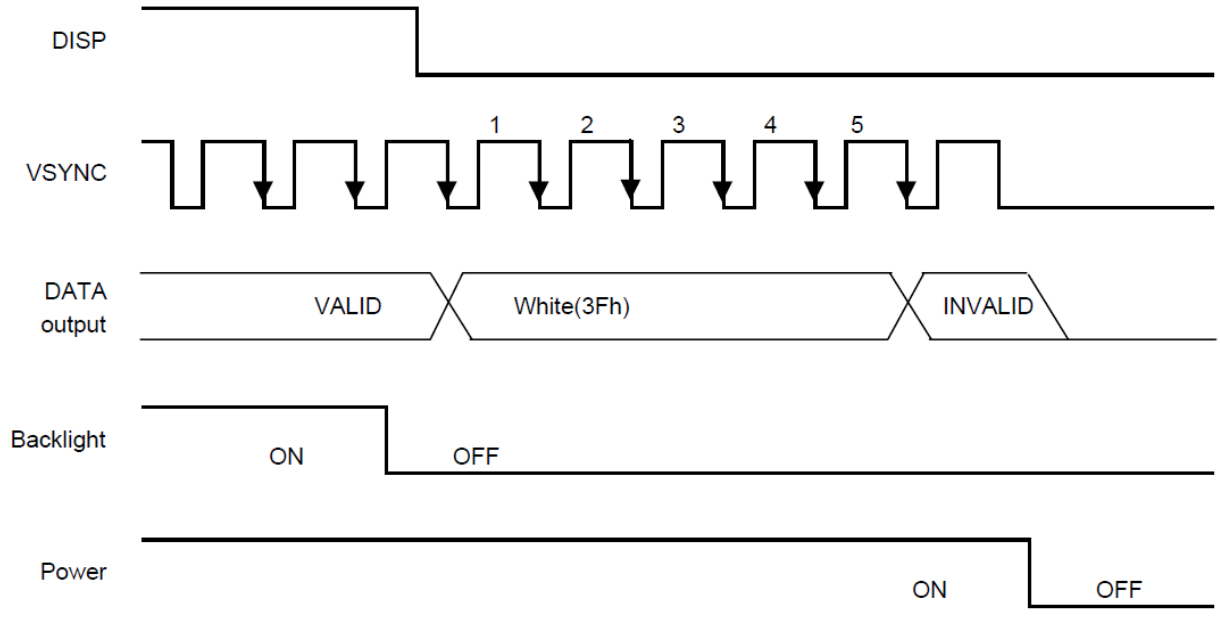


3.5.3 Display ON/OFF Sequence

After Display on, "White" data is outputted for 16-Frames first, from the falling edge of the following VSYNC signal.

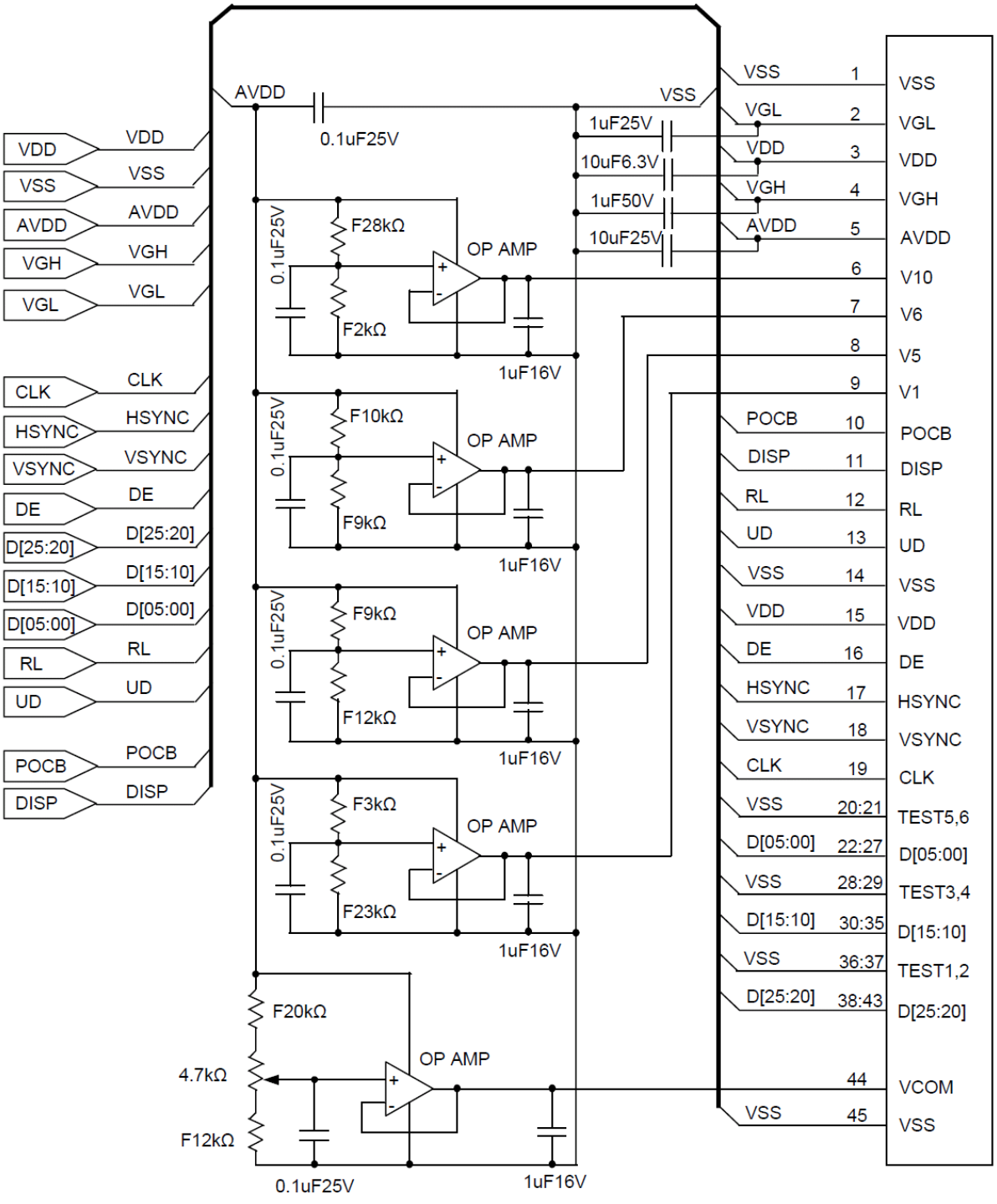


After Display off, "White" data is outputted for 5-Frames first, from the falling edge of the following VSYNC signal. Please turn off the power supply promptly after OFF of "DISP".



3.6 CIRCUIT

3.6.1 Driving circuit example (AVDD = 12.0V)



Example of OP AMP:NJM2742M

TFT LCD MODULE REFERENCE CIRCUIT

This circuit is solely for reference purpose and optimum circuit and components values may be different. User's due consideration and evaluation must be given to this circuit design and component values prior to their intended use

4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Measuring instruments: CS1000（KONICA MINOLTA), LCD7000 (OTSUKA ELECTRONICS)
EZcontrast160D（ELDIM)
Driving condition: According to “3.2 Electrical Characteristics”
Optimized VCOMDC
VLCD = Vsigpp/2
Backlight: IL = 15 mA
Measured temperature: Ta ＝ 25° C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Note
Response Time	Rise Time	TON	VLCD=0.6V→4.9V	-	-	40	ms	1	*
	Fall Time	TOFF	VLCD=4.9V→0.6V	-	-	60	ms		
Contrast Ratio	Backlight ON	CR	VLCD= 0.6V/4.9V	360	600	-		2	
	Backlight OFF			-	5.5	-			
Viewing Angle	Left	θL	VLCD= 0.6V/4.9V CR ≥ 10	80	80	-	deg	3	*
	Right	θR		80	80	-	deg		
	Up	φU		55	60	-	deg		
	Down	φD		60	65	-	deg		
V-T Threshold Voltage		V90		1.2	1.5	1.8	V	4	*
		V50		1.8	2.1	2.4	V		
		V10		2.5	2.8	3.1	V		
White V-T Curve				White V-T Curve					Reference
White Chromaticity		x	VLCD= 0.6V	White Chromaticity Range				5	
		y							
Burn-in				No noticeable burn-in image should be observed after 2hours of window pattern display.				6	
Centre Brightness			VLCD= 0.6V	385	550	-	cd/m²	7	
Brightness Distribution			VLCD= 0.6V	70	-	-	%	8	

* Measured in the form of LCD module

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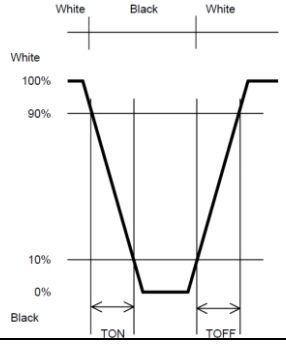
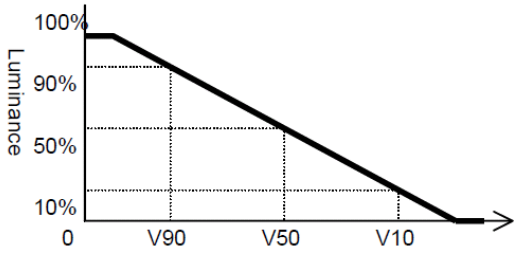
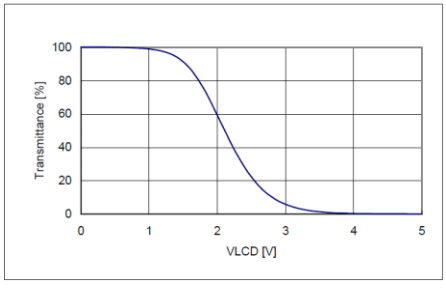
4.1.1 Test Method

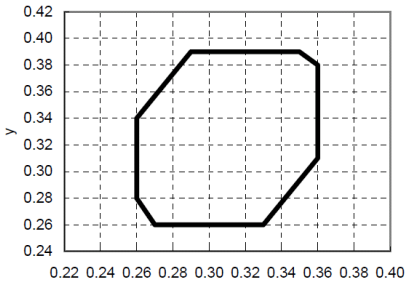
Note	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 	LCD7000	Black display VLCD=4.9V White display VLCD=0.6V TON Rise Time TOFF Fall Time
2	Contrast ratio	Measure maximum luminance Y1 (VLCD=0.6V) and minimum luminance Y2 (VLCD=4.9V) at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2 Diameter of measuring point: 8mm Ø	CS1000 LCD7000	Backlight ON Backlight OFF
3	Viewing angle Horizontal θ Vertical Ø	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10	EZcontrast160D	
4	V-T Threshold Value	Change VLCD by 0.1V step and plot the points where the luminance is 90% as V90, 50% as V50 and 10% as V10 of maximum luminance. 	LCD7000	
5	White chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system at VLCD=0.6V Colour matching faction: 2° view	CS1000	
6	Burn-in	Visually check burn-in image on the screen after 2 hours of “window display” (VLCD=0.6V/4.9V).		At optimized VCOMDC
7	Centre brightness	Measure the brightness at the centre of the screen	CS1000	
8	Brightness distribution	(Brightness distribution)= 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points	CS1000	



White V-T Curve

【White Chromaticity Range】

x	y
0.26	0.34
0.26	0.28
0.27	0.26
0.33	0.26
0.36	0.31
0.36	0.38
0.35	0.39
0.29	0.39



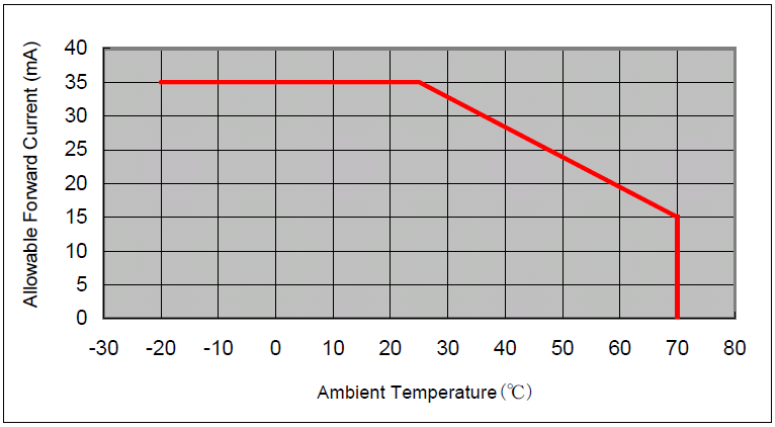
5 BACKLIGHT SPECIFICATION

5.1 LED DRIVING CONDITIONS

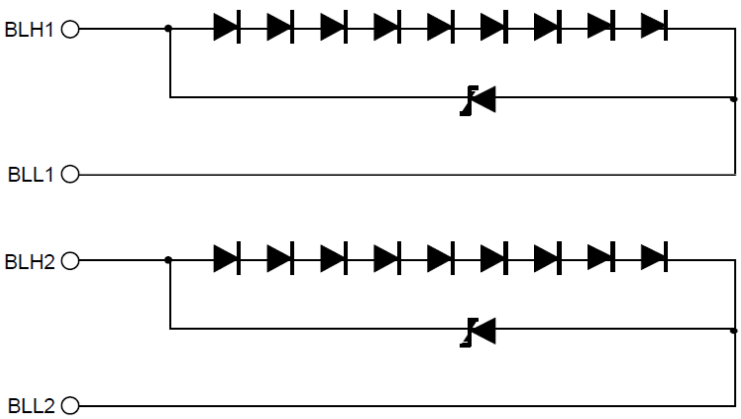
Item	Symbol	Condition	Rating			Unit	Applicable Terminal
			Min	Typ	Max		
Forward Current	IL25	Ta= 25°C	-	15.0	35.0	mA	BLH1-BLL1 BLH2-BLL2
	IL70	Ta= 70°C	-	-	15.0	mA	
Forward Voltage	VL	Ta= 25°C, IL= 15.0 mA	-	27.9	30.6	V	
Estimated Life of LED	LL	Ta= 25°C, IL= 15.0 mA Note	-	(50,000)	-	hr.	

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
  The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.



5.2 LED CIRCUIT



6 QUALITY ASSURANCE SPECIFICATION

6.1 DEFECTIVE DISPLAY AND SCREEN QUALITY

Observed TFT-LCD monitor from front during operation with the following conditions

Driving signal	Raster Pattern (RGB in monochrome, white black)
Signal condition	VLCD: 0.6, 2.4V, 4.9V (3 Steps)
Observation Distance	30cm
Illuminance	200 to 350 lx
Backlight	IL= 15 mA

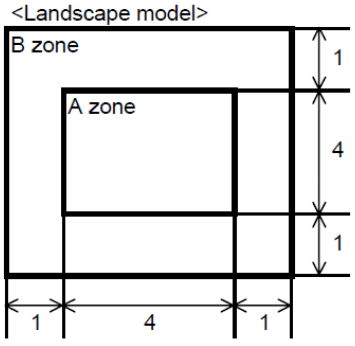
Defect item		Defect content		Criteria
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots		Not exists
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at VLCD=4.9V Low bright dot: Visible through 5% ND filter at VLCD=4.9V Dark dot: Appear dark through white display at VLCD=2.4V		Refer to table 1
Screen Quality	Dirt	Point-like uneven brightness (white stain, black stain etc)		Invisible through 1% ND filter
	Foreign particle	Point-like	0.25mm<φ	N=0
			0.20<φ≦0.25mm	N≦2
			φ≦0.20mm	Ignored
		Liner	3.0mm<length and 0.08mm<width	N=0
			length≦3.0mm or width≦0.08mm	Ignored
	Others			Use boundary sample for judgment when necessary

φ(mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more
B	2	4	4	6	Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
Total	2	4	4	7	

<Landscape model>



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1
(Refer to the left figure)

6.2 SCREEN AND OTHER APPEARANCE

Testing conditions
Illuminance 1200~2000 lx
Observation distance 30cm

Item		Criteria	Remark
Polariser	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only
S-case		No functional defect occurs	
Connector		No functional defect occurs	

6.3 DEALING WITH CUSTOMER COMPLAINTS

6.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.3.2 Handling of non-conforming displays

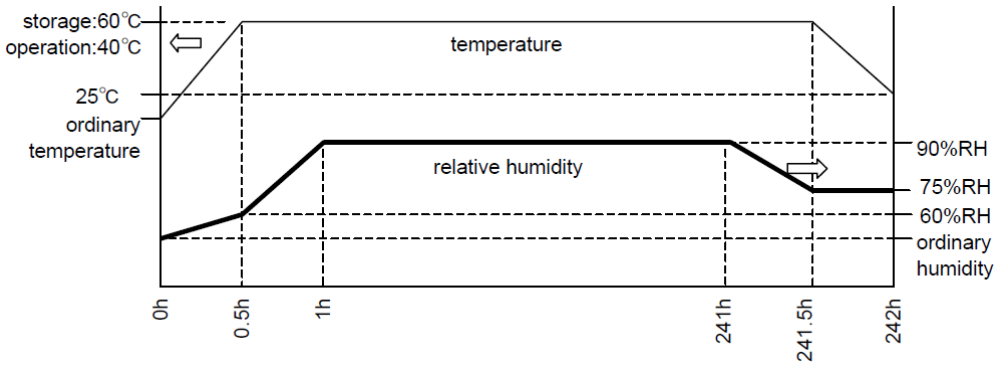
If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7 RELIABILITY SPECIFICATION

7.1 RELIABILITY TESTS

Test Item		Test Condition	Number of failures/ number of examinations
Durability Test	High Temperature Storage	Ta= 80˚C 240h	0/3
	Low Temperature Storage	Ta=-30˚C 240h	0/3
	High Temperature & High Humidity Storage	Ta= 60°C, RH= 90% Non condensing 240h	0/3
	High Temperature Operation	Top= 70°C 240h	0/3
	Low Temperature Operation	Top= -20°C 240h	0/3
	High Temperature & Humidity Operation	Top= 40°C RH= 90% 240h Non condensing	0/3
	Thermal Shock Storage	-30←→ 80°C (30 min/ 30min) 100cycles	0/3
Mechanical Environmental Test	Electrostatic Discharge Test (non operation)	Confirms to EIAJ ED-4701/300 C= 200 pF, R= 0 Ω, V= ±200V Each 3 times of discharge on and power supply and other terminals.	0/3
	Surface Discharge Test (non operation)	C= 250 pF, R= 100 Ω, V=± 12kV Each 5 times of discharge in both polarities on the centre of screen with the case grounded.	0/3
	FPC tension test (FPC of LCD only)	Pull the FPC with the force of 3N for 10 seconds in the direction -90° to its original direction	0/3
	FPC bend test (FPC of LCD only)	Pull the FPC with the force of 3N for 10 seconds in the direction -180° to its original direction. Repeat 3 times	0/3
	Vibration test	Total amplitude 1.5 mm, f= 10~55 Hz, X,Y,Z directions for each 2 hours.	0/3
	Impact test	Use original jig and make an impact with peak acceleration of 1000 m/s²for 6 ms with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-1995	0/3
Packing Test	Packing Vibration-Proof Test	Acceleration of 19.6 m/s ² with frequency of 10 → 55→ 10 Hz, X, Y, Z direction for each 30 minutes.	0/1 Packing
	Packing Drop Test	Drop from 75 cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	0/1 Packing

Note: Ta=ambient temperature Top= Panel temperature



Reliability Criteria: measure following parameters after leaving the TFT at 25°C for 24 hours or more.

Item	Standard	Remark
Display quality	No visible abnormalities shall be seen	As per Quality Assurance Specification
Contrast ratio	40 or more	Backlight ON

8 HANDLING PRECAUTIONS

Safety
If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.
If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS.
Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).