

# LIQUID CRYSTAL DISPLAY MODULE

# **Product Specification**

CUSTOMER	Standard
CUSTOMER PART NUMBER	
PRODUCT NUMBER	DBC-24032024-2A0

Product Mgr	Design Eng
Bruno Recaldini	Luo Luo
Date: 11-Jul-12	Date: 11-Jul-12

Product No. DBC-24032024-2A0 REV. 1.0	
---------------------------------------	--

Page	1 / 32	



## **TABLE OF CONTENTS**

I	<b>IVI</b> A	AIN FEATURES	4
2	MI	ECHANICAL SPECIFICATION	5
	2.1 2.2 2.3	MECHANICAL CHARACTERISTICS	6
3	EL	ECTRICAL SPECIFICATION	8
	3.1 3.2 3.3 3.4 3.5	ABSOLUTE MAXIMUM RATINGS  ELECTRICAL CHARACTERISTICS  INTERFACE PIN ASSIGNMENT  TIMING CHARACTERISTICS  INTERFACE	8 9 10
4	OP	TICAL SPECIFICATION	25
	4.1	OPTICAL CHARACTERISTICS	25
5	BA	CKLIGHT SPECIFICATION	27
	5.1 5.2	LED DRIVING CONDITIONSLED CIRCUIT	
6	QU	JALITY ASSURANCE SPECIFICATION	28
	6.1 6.2 6.3	DEFECTIVE DISPLAY AND SCREEN QUALITY	29
7	RE	LIABILITY SPECIFICATION	31
	7.1	RELIABILITY TESTS	31
8	HA	ANDLING PRECAUTIONS	32

Product No.	DBC-24032024-2A0	REV. 1.0	Page	2/32	ì



## **REVISION RECORD**

Rev.	Date	Page	Chapt.	Comment	ECN no.
1.0	11-Jul-12			First Issue	

Product No.	DBC-24032024-2A0	REV. 1.0	l
-------------	------------------	----------	---

Page	3 / 32



## 1 MAIN FEATURES

ITEM	CONTENTS
Screen Size	2.4" Diagonal
Display Format	240 x RGB x 320 Dots
N° of Colour	262k
Overall Dimensions	42.50 mm (H) x 58.50 mm (V) x 2.60 mm (D)
Active Area	36.00 mm (H) x 48.00 mm (V)
LCD Type	TFT
Mode	Sunlight Readable
Interface	CPU 16 / 18-bit
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

Product No.	DBC-24032024-2A0	REV. 1.0	
-------------	------------------	----------	--

Page	4 / 32



# **2 MECHANICAL SPECIFICATION**

## 2.1 MECHANICAL CHARACTERISTICS

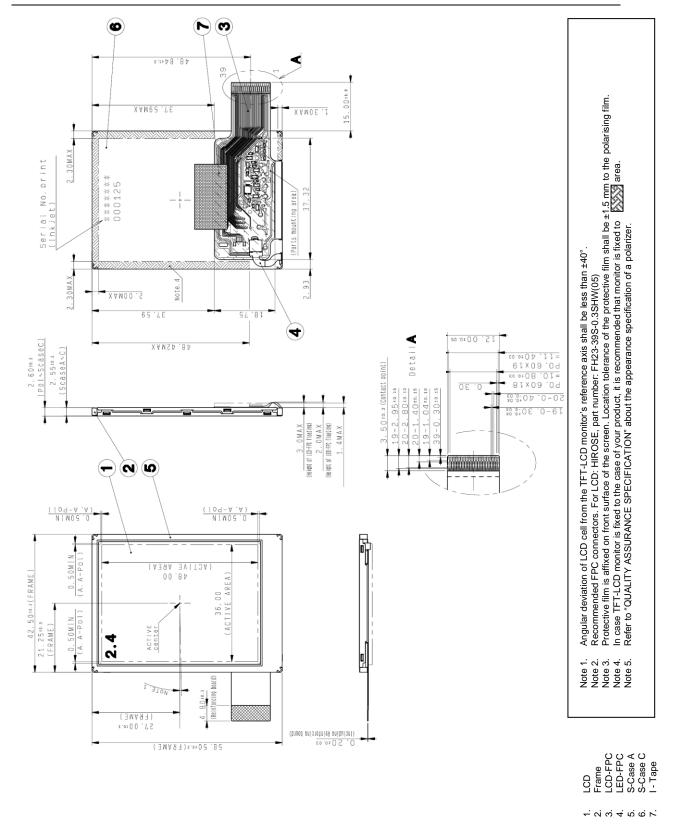
ITEM CHARACTERISTIC		UNIT
Display Format	240 x RGB x 320	Dots
Overall Dimensions 42.50 mm (H) x 58.50 mm (V) x 2.60 mm (D)		mm
Bezel Opening Area	-	mm
Active Area	36.00 mm (H) x 48.00 mm (V)	mm
Dot Pitch	50.0 (H) x RGB x 150.0 (V)	μm
Weight	13.6	g

Product No	DBC-24032024-2A0	RFV 10

Page	5 / 32



### 2.2 MECHANICAL DRAWING



 Product No.
 DBC-24032024-2A0
 REV. 1.0
 Page
 6 / 32



#### 2.3 SERIAL LABEL / PRINT

The label / print indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (4 or 5 characters), serial number (6 digits).

#### \* Label / Print Contents

#### where:

- a The least significant digit of manufacturing year
- b Manufacturing Month: Jan-A, Feb-B, Mar-C, Apr-D, May-E, Jun-F, Jul-G, Aug-H, Sep-I, Oct-J, Nov-K, Dec-L
- c Model code 24AJC → Made in Japan 24AKC → Made in Malaysia 24ALC → Made in China
- d Serial number, like "000125"

#### Examples:

Made in Japan 0K24AJC000125 means "manufactured in November 2010, model 24AJC, serial number 000125"

Made in Malaysia 0K24AKC000125 means "manufactured in November 2010, model 24AKC, serial number 000125"

Made in China 0K24ALC000125 means "manufactured in November 2010, model 24ALC, serial number 000125"

ı	Product No.	DBC-24032024-2A0	REV. 1.0	Page	7 / 32	



## **3 ELECTRICAL SPECIFICATION**

### 3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit	Applicable terminal
Supply Voltage	VCI		-0.3	4.6	V	VCI
Supply Voltage for Logic	IOVCC	Ta=25°C	-0.3	VCI	V	IOVCC
Input Voltage for Logic	VI		-0.3	IOVCC+0.3	V	RESETB, CSB, RS, WRB, DO-D17, BSO, BS1, RDB

#### 3.2 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Тур	Max	Unit	Applicable terminal	
Supply Voltage	VCI	To=25°C	2.6	2.7	3.6	V	VCI	
Supply Voltage for Logic	IOVCC	Ta=25°C	1.65	VCI	VCI	V	IOVCC	
Input Voltage for Logic	VI		0	-	IOVCC	V	RESETB, CSB, RS, WRB, DO- D17, BSO, BS1, RDB	
Input Voltage for Logic	VIH		0.7xIOVCC	-	IOVCC	V	RESETB, CSB, RS, WRB, DO-	
input voltage for Logic	VIL		0	-	0.3xIOVCC	v	D17, BSO, BS1, RDB	
Outrot Valta va fan Lasia	VOH	IOH=0.1mA	0.8xIOVCC	-	-	V	DO-D17,	
Output Voltage for Logic	VOL	IOL=0.1mA	-	-	0.2xIOVCC	V	TE	
On and the or Oursell	ICI	Colour bar display,	-	5.5	11.0	mA	VCI	
Operating Current	IOICC	still image	-	0.5	1.0	μA	IOVCC	
Standby Current	ICIs	Other input with	-	1.0	2.0	μA	VCI	
Standby Current	IOICCs constant voltage		-	6.0	25.0	μA	IOVCC	

Note: a still image (colour bar) on display, when CPU does not access the GRAM.

Product No.	DBC-24032024-2A0	REV. 1.0		Page	8 / 32	ì
-------------	------------------	----------	--	------	--------	---



### 3.3 INTERFACE PIN ASSIGNMENT

#### 3.3.1 LCM PIN ASSIGNMENT

Pin No.	Symbol	Function
1	VSS	Ground
2	VSS	Ground
3	VCI	Power supply
4	IOVCC	Power supply
5	VSS	Ground
6	RESETB	Reset signal. When RESETB is Lo, an internal reset is performed
7	CSB	Chip select signal (Active Low)
8	RS	Select register signal (Lo: index; Hi: command or display data)
9	WRB	Write strobe signal
10	VSS	Ground
11	D0	Data Bus
12	D1	Data Bus
13	D2	Data Bus
14	D3	Data Bus
15	D4	Data Bus
16	D5	Data Bus
17	D6	Data Bus
18	D7	Data Bus
19	D8	Data Bus
20	D9	Data Bus
21	D10	Data Bus
22	D11	Data Bus
23	D12	Data Bus
24	D13	Data Bus
25	D14	Data Bus
26	D15	Data Bus
27	D16	Data Bus (connect it to VSS when using 16-bit interface)
28	D17	Data Bus (connect it to VSS when using 16-bit interface)
29	VSS	Ground
30	BS0	Interface mode selection
31	BS1	Interface mode selection
32	RDB	Read strobe signal (connect it to IOVCC when not used)
33	NC	Open
34	NC	Open
35	NC	Open
36	NC	Open
37	TE	Frame head output pulse (connect it to IOVCC when not used)
38	BLH	LED drive power source (Anode side)
39	BLL	LED drive power source (Cathode side)

Recommended connector: Hirose Electric FH23 series [FH23-39S-0.3SHW(05)]

As FCB cable has gold plated terminals, gilt finish contact shoe connector is recommended.

Product No. DBC	-24032024-2A0	REV. 1.0		Page	9 / 32	l
-----------------	---------------	----------	--	------	--------	---



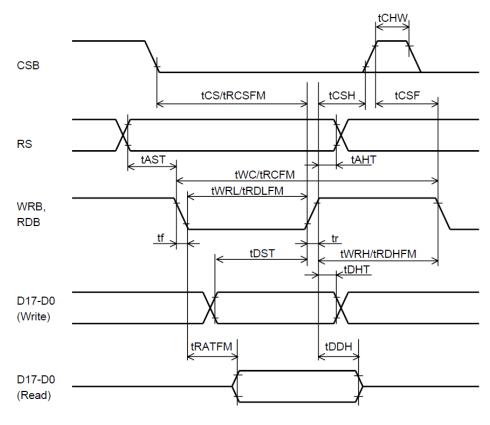
### 3.4 TIMING CHARACTERISTICS

## 3.4.1 AC Timing Characteristics

Unless otherwise noted, Ta=25°C, VCI=IOVCC=2.7V, VSS=0V

			Ra	ting	
Item	Symbol	Condition	MIN	MAX	Unit
Address setup time	tAST	RS	10	-	ns
Address hold time	that	RS	10	-	ns
CSB high level pulse width	tCHW	CSB	0	-	ns
CSB setup time	tCS	CSB-WRB	35	-	ns
CSB setup time	tRCSFM	CSB-WRB	180	-	115
CSB wait time	tCSF	CSB	10	-	ns
CSB hold time	tCSH	CSB	10	-	ns
WRB bus cycle time	tWC	WRB	100	-	ns
WRB high level pulse width	tWRH	WRB	15	-	ns
WRB low level pulse width	tWRL	WRB	20	-	ns
RDB bus cycle time	tRCFM	WRB	250	-	ns
RDB high level pulse width	tRDHFM	WRB	15	-	ns
RDB low level pulse width	tRDLFM	WRB	180	-	ns
WRB data setup time	tDST	D17-D0	10	-	ns
WRB data hold time	tDHT	D17-D0	10	-	ns
RDB access time	tRATFM	D17-D0	-	340	ns
RDB output disable time	tDDH	D17-D0	20	80	ns
Input signal rising time	tr	-	-	15	ns
Input signal falling time	tf	-	-	15	ns

The switching voltage is set at 30% to 70% of IOVCC voltage





## 3.5 INTERFACE

	Inc	lex/			(	GRAN	1 Write	9		
	Com	mand				CI	⊃U			
Bus Width	W	rite		18bit	16bit	16	bit		8bit	
Transferring Me	thod		•	18	16	16	+2		6+6+6	6
Width of data of	f 1 pixel			18	16	1	8		18	
BS1		*		Н	L	I			Н	
BS0		*		L	L	_	1		Н	
D17				R5						
D16				R4						
D15				R3	R5/R0	R5				
D14				R2	R4	R4				
D13				R1	R3	R3				
D12				R0	R2	R2				
D11				G5	R1	R1				
D10				G4	G5	R0				
D9				G3	G4	G5				
D8				G2	G3	G4				
D7	ID7	RB7		G1	G2	G3		R5	G5	B5
D6	ID6	RB6		G0	G1	G2		R4	G4	В4
D5	ID5	RB5		B5	G0	G1		R3	G3	В3
D4	ID4	RB4		B4	B5/B0	G0		R2	G2	В2
D3	ID3	RB3		B3	B4	B5		R1	G1	B1
D2	ID2	RB2		B2	В3	B4		R0	G0	В0
D1	ID1	RB1		B1	B2	В3	B1			
D0	ID0	RB0		В0	B1	B2	В0			

Please connect any unused terminal of D0-D17 to VSS

			_		
Product No	DBC-24032024-2A0	RFV 1.0		Page	11 / 32



### 3.5.1 REGISTER LIST

	Register	D17-8	D7	D6	D5	D4	D3	D2	D1	D0			
R01h	Display Mode control	*	*	*	*	*	IDMON	INVON	NORON	<b>PTLON</b>			
1	initial (0006h)						0	1	1	0			
	recommend (0006h)						0	1	1	0			
R02h	Column address start 2	*				SC[	15:8]						
1	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R03h	Column address start 1	*				SC	[7:0]						
1	initial (0000h)		0	0	0	0	0	0	0	0			
1	recommend (0000h)		0	0	0	0	0	0	0	0			
R04h	Column address end 2	*				ECI.	15:8]						
1	initial (0000h)		0	0	0	0	0	0	0	0			
1	recommend (0000h)		0	0	0	0	0	0	0	0			
R05h	Column address end 1	*				ECI	[7:0]						
1	initial (00EFh)		1	1	1	0	1	1	1	1			
1	recommend (00EFh)		1	1	1	0	1	1	1	1			
R06h	Row address start 2	*				SPI <sup>-</sup>	15:8]						
	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R07h	Row address start 1	*				SPI	7:0]						
	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R08h	Row address end 2	*					15:8]						
110011	initial (0001h)		0	0	0	0	0	0	0	1			
1	recommend (0001h)		0	0	0	0	0	0	0	1			
R09h	Row address end 1	*	Ť				7:0]						
1.0011	initial (003Fh)		0	0	1	1	1	1	1	1			
	recommend (003Fh)		0	0	1	1	1	1	1	1			
R0Ah	Partial area start row 2	*			•	PSLI	15:8]						
107111	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R0Bh	Partial area start row 1	*	- ŭ	<u> </u>	<u> </u>		[7:0]		<u> </u>				
I NOBII	initial (0000h)		0	0	0	0	0	0	0	0			
1	recommend (0000h)		0	0	0	0	0	0	0	0			
R0Ch	Partial area end row 2	*					[15:8]						
110011	initial (0001h)		0	0	0	0	0	0	0	1			
	recommend (0001h)		0	0	0	0	0	0	0	1			
R0Dh	Partial area end row 1	*	U	U	U		[7:0]	U	U				
INODII	initial (003Fh)		0	0	1	1	1	1	1	1			
	recommend (003Fh)		0	0	1	1	1	1	1	1			
R0Eh	Vertical Scroll Top fixed area 2	*		J			15:8]			•			
IXOLII	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R0Fh	Vertical Scroll Top fixed area 1	*	- 0	J	J		[7:0]	0	J	3			
130111	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R10h	Vertical Scroll height area 2	*	0		J		[15:8]	0	0	3			
13 1011			0		0			0		1			
	initial (0001h) recommend (0001h)		0	0	0	0	0	0	0	1			
R11h	Vertical Scroll height area 1	*	U	U	U		.[7:0]	U	U				
IXTIII				1					I 0	0			
	initial (0040h) recommend (0040h)		0	1	0	0	0	0	0	0			
Diah		*	U		U			U	U	U			
R12h	Vertical Scroll Button area 2			I ^			[15:8]	_	I ^				
	initial (0000h) recommend (0000h)		0	0	0	0	0	0	0	0			
			U	0	0	U	0	0	U	0			

			_		
Product No.	DBC-24032024-2A0	REV. 1.0		Page	12 / 32



	Register	D17-8	D7	D6	D5	D4	D3	D2	D1	D0			
R13h	Vertical Scroll Button area 1	*				BFA	[7:0]						
	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R14h	Vertical Scroll Start address 2	*		_	_		[15:8]			_			
	initial (0000h) recommend (0000h)		0	0	0	0	0	0		0			
R15h	Vertical Scroll Start address 1	*	U	U	U		P[7:0]	U	U	U			
1311	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0000h)		0	0	0	0	0	0		0			
R16h	Memory Access control	*	MY	MX	MV	*	BGR	*		*			
	initial (0000h)		0	0	0		0						
	recommend (0008h)		0	0	0		1						
R18h	Gate Scan control	*	*	*	*	*	*	*		SM			
	initial (0000h)								0	0			
	recommend (0001h)								0	1			
R19h	OSC Control 1	*		CAD	J[3:0]		C	UADJ[2:	OSC_ EN				
	initial (0086h)		1	0	0	0	0	1		0			
	recommend (0087h)		1	0	0	0	0	1	1	1			
R1Ah	OSC Control 2	*	*	*	*	*	*	*	*	OSC_ TEST			
	initial (0000h)								L_ON	0			
	recommend (0000h)									0			
R1Bh	Power Control 1	*	GAS ENB	*	*	PON	DK	XDK	TRI	STB			
	initial (0000h)		0			0	0	0		0			
DAOL	recommend (0014h)	*	0 *	*	*	1 *	0	1		0			
R1Ch	Power Control 2 initial (0004h)		^	~			^	1		0			
	recommend (0004h)							1		0			
R1Dh	Power Control 3	*	*	*	*	*	*						
	initial (0004h)							1		0			
	recommend (0005h)							1		1			
R1Eh	Power Control 4	*	*	*	*	*	*		VC3[2:0]				
	initial (0000h)							0		0			
	recommend (0000h)							0		0			
R1Fh	Power Control 5	*	*	*	*	*							
	initial (0006h) recommend (0007h)						0	1		1			
R20h	recommend (0007h) Power Control 6	*		DTI	3:0]		*	*		*			
1\ZUII	initial (0060h)		0	БI <u>[</u>	3:0] 1	0							
	recommend (0000h)		0	0	0	0							
R21h	Power Control 7	*	*	*		[1:0]	*	*	FS0	[1:0]			
	initial (0010h)				0	1				0			
	recommend (0010h)				0	1				0			
R22h	Write Data				G	RAM Wr	ite						
	initial (0000h)												
	recommend (0000h)												
R23h	Cycle Control 1	*					C[7:0]						
	initial (0095h)		1	0	0	1	0	1		1			
D24h	recommend (0095h)	*		0	U		0		U	1			
R24h	Cycle Control 2 initial (0095h)		1	0	0		C[7:0]	1		1			
	initial (0095h) recommend (0095h)		1	0	0	1	0	1	0	1			
	recommend (0035H)			U	U		U		U				

			_		
Product No.	DBC-24032024-2A0	REV. 1.0		Page	13 / 32



R25h		Register	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	
R26h	R25h	Cycle Control 3	*				I_DC	[7:0]		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		
R26h				1	1	1	1	1	1	1	1	
R2Ph				•			1		•			
R27h	R26h		*	PT[	1:0]	GON	DTE	D[		*	*	
R27h												
R28h					_	•		1	•			
R28h	R27h		*	*	*	*	*					
R28h												
Right	Dool		+			+	+	U		•	U	
R29h	R28h		,	^	,	,	^	•			0	
R29h								100000000000000000000000000000000000000		1		
R2Ah	D20h		*	*	*	*	*	U		D[3·0]		
Real   Display Control 5	K29II							0			0	
R2Ah												
R2Bh	R2Ah		*	*	*	*	*					
R2Bh	1 (2)							0			0	
R2Bh												
RZBh						PI F	PRF					
R2Ch	R2Bh	Power Control 11	*	*	*				BLANK_	_DIV[3:0]		
R2Ch	l 1	initial (0000h)						0	0	Ω	Ω	
R2Ch												
R2Dh	R2Ch		*	*	*				I BF	P[3:0]	-	
R2Dh	l 1							0			0	
R2DII									0	0		
R35h	R2Dh	Display Control 7	*	*	*	*	*		I_FF	[3:0]		
R35h		initial (0002h)						0	0	1	0	
R36h		recommend (0008h)						1	0	0	0	
R36h	R35h		*				EQS	[7:0]				
R36h												
R30h	_			0	0	0	_	•	0	0	1	
R37h	R36h		*									
R37h												
R38h   RGB interface control 2   *   *   *   *   *   *   *   *   *	D071							1			1	
R38h   RGB interface control 1   *   *   *   *   *   *   *   *   RGB   EN   DPL   HSPL   VSPL   EPL	R3/h		Ŷ	^	^			•			•	
R38h   RGB interface control 1   *   *   *   *   *   RGB_EN   DPL   HSPL   VSPL   EPL												
R38h   RGB Interface control		recommend (0000m)				U		U	U	U	U	
R39h   RGB interface control 2   *   DOTCLK_DIV[7:0]	R38h	RGB interface control 1	*	*	*	*		DPL	HSPL	VSPL	EPL	
R39h   RGB interface control 2   *   DOTCLK_DIV[7:0]	<b>.</b> .	: ::: (00001)						•		0	•	
R39h   RGB interface control 2   *   DOTCLK_DIV[7:0]									_			
R3Ah   Cycle Control 1   *   N_RTN[3:0]   *   N_NW[2:0]	Danh		*							U	U	
R3Ah	179911			0	0					0	0	
R3Ah         Cycle Control 1         *         N_RTN[3:0]         *         N_NW[2:0]           initial												
R3Bh   Cycle Control 2   * PI_RTN[3:0]   * PI_NW[2:0]     R3Ch   Cycle Control 3   * I_RTN[3:0]   * I_NW[2:0]     Initial (0001h)	R3Ah		*	,			,	_				
R3Bh   Cycle Control 2   * PI_RTN[3:0]   * PI_NW[2:0]     Initial (0001h)   1 0 1 0 0 0 1     R3Ch   Cycle Control 3   * I_RTN[3:0]   * I_NW[2:0]     Initial (00F0h)   1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	100/111	•		0			n					
R3Bh         Cycle Control 2         *         PI_RTN[3:0]         *         PI_NW[2:0]           initial         (0001h)         0         0         0         0         0         1           recommend         (00A1h)         1         0         1         0         0         0         1           R3Ch         Cycle Control 3         *         I_RTN[3:0]         *         I_NW[2:0]           initial         (00F0h)         1         1         1         1         0         0         0									_			
initial (0001h)	R3Bh		*			•		*				
recommend (00A1h)		•		0			0				_	
R3Ch		()				1						
initial (00F0h) 1 1 1 1 0 0 0	R3Ch		*		I_RT	N[3:0]		*		_NW[2:0	]	
	H	-		1		1	1				_	
						1						

			_		
Product No.	DBC-24032024-2A0	REV. 1.0		Page	14 / 32



	Register	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R3Dh	Cycle Control 4	*	*	*	DIV	I[1:0]	DIV_I	PI[1:0]	DIV	N[1:0]
	initial (0000h)				0	0	0	0	DIV_N 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
	recommend (0000h)				0	0	0	0	0	0
R3Eh	Cycle Control 5	*				SON	I[7:0]			
	initial (0038h)		0	0	1	1	0] DIV_PI[1:0] DIV 0 0 0 0 0 0 0 0 0 SON[7:0] 1 1 0 0 0 GDON[7:0] 0 0 0 1 1 0 GDOF[7:0] 1 1 0 0 0 The state of the	0	0	
	recommend (002Dh)		0	0	1	0	1	1	0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
R40h	Cycle Control 6	*				GDO	N[7:0]			
	initial (0003h)		0	0	0				1	1
	recommend (0003h)		0	0	0			0	1	1
R41h	Cycle Control 7	*				GDO	F[7:0]			
	initial (00F8h)		1	1	1					0
	recommend (00CCh)		1	1	0	0	1	1	0	0
R42h	BGP Control	*	*	*	*	VBGP_ OE		BGF	P[3:0]	
	initial (0008h)					0	1		0	0
	recommend (0008h)							_		0
R43h	VCOM Control 1	*	VCOMG	*	*	*	*	*	*	*
	initial (0080h)		1							
	recommend (0080h)		1							
R44h	VCOM Control 2	*	*							
	initial (005Ah)			1	0					0
·	recommend (007Fh)	*	*	1 *	1 *	1		•		1
R45h	VCOM Control 3	*	*	*	*					
	initial (0011h)							0		1
D 401	recommend (0014h)	*	0051		000450.03					0
R46h	r Control 1	,	GSEL	•	CP1[2:0]		r	0		
	initial (0000h) recommend (0086h)		0	0	0					0
R47h	r Control 2	*	*	U	CN1[2:0]		*	•		
134711	initial (0000h)			0	0					0
	recommend (0060h)			1	1					0
R48h	r Control 3	*	*	•	NP1[2:0]		*			
	initial (0000h)			0	0			0		0
	recommend (0001h)			0	0					1
R49h	r Control 4	*	*		NP3[2:0]	_	*		_	•
	initial (0000h)			0	0			0		0
	recommend (0067h)			1	1	0		1		1
R4Ah	r Control 5	*	*		NP5[2:0]		*		NP4[2:0	]
	initial (0000h)			0	0	0		0		0
	recommend (0046h)			1	0	0		1		0
R4Bh	r Control 6	*	*		NN1[2:0]		*		NN0[2:0	]
	initial (0000h)			0	0	0		0		0
	recommend (0013h)			0	0	1		0	1	1
R4Ch	r Control 7	*	*		NN3[2:0]		*		NN2[2:0	]
	initial (0000h)			0	0	0		0	0	0
	recommend (0001h)			0	0	0		0	0	1
R4Dh	r Control 8	*	*		NN5[2:0]		*		NN4[2:0	]
	initial (0000h)			0	0	0		0	0	0
	recommend (0067h)			1	1	0		1	1	1
R4Eh	r Control 9	*	CGMF	P1[1:0]	CGMF	P0[1:0]		OPO	[3:0]	
	initial (0000h)		0	0	0	0	0	0	0	0
	recommend (0000h)		0	0	0	0	0	0	0	0

			_		
Product No.	DBC-24032024-2A0	REV. 1.0		Page	15 / 32



	Register	D17-8	D7	D6	D5	D4	D3	D2	D1	D0			
R4Fh	r Control 10	*	CGMP3	CGMP2	*			OP1[4:0]					
	initial (0000h)		0	0	0	0	0	0	0	0			
	recommend (0013h)		0	0	0	1	0	0	0] 0 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1			
R50h	r Control 11	*		V1[1:0]		N0[1:0]	•		0] 0 0 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0				
l 1	initial (0000h) recommend (0002h)		0	0	0	0	0	0	4:0]  0 1 1 0N0[3:0]  0 1 4:0]  0 0 1 4:0]  0 0 0 1 1 1 VPP_S EL  0 0 0 0 1 1 TRI[ 0 0 0 ADJ[3:0] 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0			
R51h	r Control 12	*		CGMN2	*		_	ON1[4:0]	-				
	initial (0000h)		0	0	0	0	0	0	0]	0			
	recommend (0000h)		0	0	0	0	0	0	0	0			
R52h	OTP Control 1	*					ASK[7:0]						
	initial (0000h)		0	0	0	0	0	0		0			
R53h	recommend (0000h) OTP Control 2	*	0	0	0	OTD IN	0 DEX[7:0]	0	U	0			
Koon	initial (00FFh)		1	1	1	1 1	DΕλ[7.0]	1	1	1			
1 1	recommend (00FFh)		1	1	1	1	1	1		1			
R54h	OTP Control 3	*	OTP_L OAD_D ISABLE	_DISAB	OTP_ POR	OTP_ PWE	OTP_ PTM	0	_	OTP_ PROG			
	initial (0008h)		0	0	0	0	1			0			
R64h	recommend (0008h)	*	0	0	0	0	1		0	0			
K04n	initial (0000h)		0	0	0	0	[7:0] 0	0	Λ	0			
1 1	recommend (0000h)		0	0	0	0	0	0		0			
R65h	Internal Use 17	*	*				ID2[6:0]						
	initial (0000h)			0	0	0	0	0		0			
	recommend (0000h)			0	0	0	0	0	0 0				
R66h	Internal Use 18	*					[7:0]						
1 1	initial (0000h) recommend (0000h)		0	0	0	0	0	0		0			
R67h	Internal Use 19	*	U	U	U		[7:0]	U	U	0			
	initial (0047h)		0	1	0	0	0	1	1	1			
	recommend (0047h)		0	1	0	0	0	1	1	1			
R70h	Internal Use 28	*	*	GS	SS	TE MODE	TEON	(	CSEL[2:0	)]			
	initial (0006h)			0	0	0	0	1		0			
R72h	recommend (0066h)  Data control	*	*	*	•	1[1:0]	*	*	000000000				
137211	initial (0000h)				0	0							
	recommend (0000h)				0	0				0			
R90h	Display Control 8	*				SAF	[7:0]						
	initial (000Ah)		0	0	0	0	1	0		0			
DO41	recommend (007Fh)	*	0	1	1	1 CEN C	1	1	1	1			
R91h	Display Control 11 initial (0014h)		0	0	0	GEN_C	0FF[7:0]	1	0	0			
	recommend (0014h)		0	0	0	1	0	1		0			
R93h	OSC Control 3	*	*	*	*	*							
1 1	initial (000Fh)						1	1		1			
$\Box$	recommend (000Fh)						1	1	1	1			
R94h	SAP Idle mode	*			_		_I[7:0]						
l	initial (000Ah) recommend (000Ah)		0	0	0	0	1	0		0			
R95h	DCCLK SYNC TO CL1	*	*	*	*	*	*	*		DCCLK _SYNC			
	initial (0000h)									0			
L Daa:	recommend (0001h)			_		4.	at.	_		1			
R96h	TEST1 initial (0000h)	*	0	*	*	0	*	*	· 0	TEST1			
	recommend (0000h)		0	0	0	0	0	0	0	0			
	(000011)		_		_								

Product No. DBC-24032024-2A0 REV. 1.0	Page	16 / 32
---------------------------------------	------	---------



#### 3.5.2 SEQUENCE

# 3.5.2.1 Power ON Sequence

Function				_									
Walt 1 to see or more   RESETB=0   Walt 10 usec or more   RESETB=0   Walt 10 usec or more   RESETB=1   Walt 120 msec or more   REST1 setting   Section   REST3   R96h   O1h   O   O   O   O   O   O   O   O   O			Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
RESETBED		RESETB=1											
Walt 10 Usec or more   RESTTS =   Walt 120 Insec or more   REST   R96h   O1h   O   O   O   O   O   O   O   O   O													
RESETB=1		RESETB=0											
Valid 20 mase or more   Valid 30 mase or more   Valid 40 mase or more   Valid 50 mase or more   Vali		wait 10 usec or more											
TEST1 setting		RESETB=1											
TEST1 setting		wait 120 msec or more											
OSC control   Setting	TEST1 setting			01h	*	0	0	0	0	0	0	0	1
Setting   Wait 10 msec or more   Display OFF   Display Control 1   R26h   80h   " PT[1:0]   GON   DTE   D[1:0]   "   "					*		CAL	J[3·0]		CI	UADJI2	·01	OSC
Name				• • • • • • • • • • • • • • • • • • • •			0, 12	0[0.0]			o, .20[2		_
Display OFF   Display Control   R26h   80h   * PT[1:0]   GON   DTE   D[1:0]   *   TRI   DISPLAY CONTROL   R26h   80h   * PT[1:0]   GON   DTE   D[1:0]   *   TRI   DISPLAY CONTROL   R18h   Ch   SAS   * PON   DK   XDK   VLCD   STB   R18h   Ch   SENB   Ch   Ch   STB   R18h   Ch   SENB   Ch   Ch   Ch   STB   R18h   Ch   SENB   Ch   Ch   Ch   Ch   Ch   Ch   Ch   C						1	0	0	0	0	1	1	
Display OFF setting   Setting   Power Control 1   R26h   80h   Power Control 1   R18h   OCh   GAS   PON   DE   D(1:0)   Power Control 1   R43h   OCh   GAS   PON   DE   D(1:0)   Power Control 1   R43h   OCh   GAS   PON   DE   D(1:0)   POwer Control 1   R43h   OCh   Power Control 2   R20h   OCh   Power Control 3   R45h   OCh   Power Control 5   R18h   OCh   Power Control 6   R20h   OCh   Power Control 7   R18h   OCh   Power Control 8   OCh   Och		wait 10 msec or more						-	-		<u> </u>	'	<u> </u>
Power Control 1	Display OFF		Doch	90h	*	TTO	1.01	CON	DTE	DI:	1.01	*	*
Power Control 1		Display Control 1	1\2011	8011								0	0
Power control   R15h   OCh   ENB   OCh	Setting	Dayyan Cantual 1	DADE	004	*		_		_			_	_
VCOM Control 1		Power Control 1	KIBN	UCh					PON	DK	XDK	1	
VCOM Control 1									•		_		
Power supply setting   Power Control 6								0	Ü			0	
Power Supply setting   Power Control 6   R20h   O0h   BT[3:0]   Power Control 5   R1Fh   O7h   Power Control 6   R20h   O7h   Power Control 7   R21h   O7		VCOM Control 1	R43h	00h	*		*	*	*	*	*	*	*
Power Supply setting   Power Control 6													
Setting   Power Control 5						0		_	0		_		
Initializing	Power supply	Power Control 6	R20h	00h	*		ВТ	[3:0]		*	*	*	*
VCOM Control 2						0	0	0	0	0	0	0	0
VCOM Control 2	initializing	Power Control 5	R1Fh	07h	*	*	*	*	*		VRH	H[3:0]	
VCOM Control 3						0	0	0	0	0	1	1	1
VCOM Control 3		VCOM Control 2	R44h	7Fh	*	*			\	/CM[6:0	01		
Power Control 3						0	1	1			_	1	1
Power Control 3		VCOM Control 3	R45h	14h	*	*	*	*		\	VDVI4:0	01	
Power Control 3						0	0	0	1				0
Power Control 4		Power Control 3	R1Dh	05h	*				-				
Power Control 4   R1Eh   00h   * * * * * * * * * * * * VC3[2:0]		1 01101 00111101 0		0011		0	0	0	0	0			_
Power supply operation start setting   Power Control 2   R1Ch   O4h   * * * * * * * * * * * * * * * * * *		Power Control 4	P1Fh	00h	*		_	*	_				
Power control 2		1 Ower Control 4	IXILII	0011		0	0	0	0	0			
Power Control 2	Dower cupply	Power Central 2	D1Ch	04h	*			_			0	_	
Start setting		Fower Control 2	KICII	0411		0	0	0	0	0	-1		
ENB	· ·	Dayyar Cantral 1	D1Db	1.4h	*		*	*					
Wait 40 msec or more   VCOM Control 1   R43h   80h   VCOM   VCO	Start Setting	Power Control 1	KIDII	1411					FOIN	DK	VDK		
Wait 40 msec or more   VCOM Control 1							_		4	_	4		
VCOM Control 1						U	U	U	1	U	1	U	U
Power control setting			D 461	0.01									
Power control setting		VCOIVI Control 1	R43h	80h			*	*		*	*	*	_ *
Power control setting							_		_				
Cycle Control 1										0			0
Cycle Control 1			R42h	08h	*	*	*	*	VBGP		BGF	2[3:0]	
Cycle Control 1         R23h         95h         *         N_DC[7:0]           1         0         0         1         0         1         0         1           Cycle Control 2         R24h         95h         *         PI_DC[7:0]	setting												
Cycle Control 2						0	0	0	_		0	0	0
Cycle Control 2         R24h         95h         *         PI_DC[7:0]           Cycle Control 3         R25h         FFh         *         I_DC[7:0]           1         2         1         1         1		Cycle Control 1	R23h	95h	*				N_D	C[7:0]			
Cycle Control 3						1	0	0	-		1	0	1
Cycle Control 3		Cycle Control 2	R24h	95h	*				PI_D	C[7:0]			
Power Control 7   R21h   10h   * * * * FS1[1:0] * * * FS0[1:0]						1	0	0			1	0	1
Power Control 7   R21h   10h   * * * * FS1[1:0] * * * FS0[1:0]		Cycle Control 3	R25h	FFh	*				I DO	[7:0]			
Power Control 7		•				1	1	1			1	1	1
Power Control 11   R2Bh   00h   *   *   *   PI_PRE_   BLANK_DIV[3:0]   REFRESH[1:0]		Power Control 7	R21h	10h	*	*	*	FS1	[1:0]	*	*	FSO	
Power Control 11						0	0			0	0		
REFRESH[1:0]		Power Control 11	R2Bh	00h	*								
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		. Office Control 11	1,2011	5511								, , [0.,	~]
DCCLK SYNC TO CL1 R95h 01h * * * * * * * * * * DCCLF _SYNC										0	0	0	0
0 0 0 0 0 0 1			DOEL	016	*	*							
0 0 0 0 0 0 1		DOOLK STNC TO CLT	Real	UIN						-			1
							_	_	_	_	_	_	
Product No. DBC-24032024-2A0 PEV 1.0 Dogo 17 / 22						U	U	U	U	U	U	U	1
	Droduct No.	DDC 240	33034	210	DEV	/ 1 0					Dogo	17	7/22



	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control	OSC Control 2	R1Ah	00h	*	*	*	*	*	*	*	*	osc_
setting												TEST
					0	0	0	0	0	0	0	0
	OSC Control 3	R93h	0Fh	*	*	*	*	*		RAD	J[3:0]	
					0	0	0	0	1	1	1	1
	Internal Use 28	R70h	66h	*	*	GS	SS	TE	TEON	C	SEL[2:	0]
								MODE				
					0	1	1	0	0	1	1	0
	Gate Scan control	R18h	01h	*	*	*	*	*	*	*	SCROL	1
											L_ON	
					0	0	0	0	0	0	0	1
r control setting	r Control 1	R46h	86h	*	GSEL		CP1[2:0				CP0[2:0	
	0 / 10	D 471	001	*	1	0	0	0	0	1	1	0
	r Control 2	R47h	60h	*			CN1[2:0	-			CN0[2:0	-
		D 401-	041-	*	0	1	1	0	0	0	0	0
	r Control 3	R48h	01h				NP1[2:0				NP0[2:0	-
	n Cantual 4	D40h	675	*	0	0	0	0	0	0	0 NP2[2:0	1
	r Control 4	R49h	67h			1	NP3[2:0	0	0			-
	r Control 5	R4Ah	46h	*	0		1 NDETO-0	_	*	1	1	1
	r Control 5	K4An	400	-		1	NP5[2:0	0		1	NP4[2:0	
	r Control 6	R4Bh	126	*	0		0 NN1[2:0	_	0		1 NN0[2:0	0
	r Control 6	K4DII	13h		0	0	0	י <u>י</u> 1	0	0	1	رب 1
	r Control 7	R4Ch	01h	*	*	_	NN3[2:0		*		NN2[2:0	
	r Control 7	K4Cn	UIN		0	0	0	0	0	0	0	رر 1
	r Control 8	R4Dh	67h	*	*	_	NN5[2:0	_	*		NN4[2:0	
	r Control 6	K4DII	6/11		0	1	1 1	0	0	1	1	رب 1
	r Control 9	R4Eh	00h	*		21[1:0]		P0[1:0]	U		0[3:0]	
	1 Control 9	K4EII	0011		0	0	0	0	0	0	0	0
	r Control 10	R4Fh	13h	*		CGMP2		0	_	OP1[4:0		- 0
	1 Control 10	114111	1311		0	0	0	1	0	0	ני 1	1
	r Control 11	R50h	02h	*		V1[1:0]		V0[1:0]	-		0[3:0]	-
	1 Control 11	110011	0211		0	0	0	0	0	0	1	0
	r Control 12	R51h	00h	*		CGMN2			_	ON1[4:0		U
	1 0011101 12	110111	0011		0	0	0	0	0	0	0	0
RGB interface	RGB interface	R38h	00h	*	*	*	*	RGB_	DPL	HSPL		
control setting	control 1							EN				
					0	0	0	0	0	0	0	0
	RGB interface	R39h	00h	*			D	OTCLK	DIV[7:	:01		
	control 2				0	0	0	0	0	0	0	0
Display control	Display Control 2	R27h	02h	*	*	*	*	*		N_BI	P[3:0]	
setting					0	0	0	0	0	0	1	0
	Display Control 3	R28h	03h	*	*	*	*	*		N_F	P[3:0]	
					0	0	0	0	0	0	1	1
	Display Control 4	R29h	08h	*	*	*	*	*		PI_B	P[3:0]	
					0	0	0	0	1	0	0	0
	Display Control 5	R2Ah	08h	*	*	*	*	*		PI_F	P[3:0]	
					0	0	0	0	1	0	0	0
	Display Control 6	R2Ch	08h	*	*	*	*	*		I_BF	[3:0]	
					0	0	0	0	1	0	0	0
	Display Control 7	R2Dh	08h	*	*	*	*	*		I_FF	[3:0]	
					0	0	0	0	1	0	0	0
	Display Control 9	R35h	09h	*				EQS	[7:0]			
					0	0	0	0	1	0	0	1
	Display Control 10	R36h	09h	*				EQP	[7:0]			
					0	0	0	0	1	0	0	1
	Display Control 11	R91h	14h	*				GEN_C	FF[7:0	]		
1					0	0	0	1	0	1	0	0
	Display Control 12	R37h	00h	*	*	*	PTG	[1:0]			[3:0]	

Product No.	DBC-24032024-2A0	REV. 1.0	Page	18 / 32



	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Display control	Display Mode control	R01h	06h	*	*	*	*	*		INVON		
setting		110111	0011		0	0	0	0	0	1	1	0
Johnson	Cycle Control 1	R3Ah	A1h	*			N[3:0]		*		_NW[2:	
	Cycle Control 1	INSAII	AIII		1	0	1	0	0	0	_1400[2.	1
	Cycle Control 2	R3Bh	A1h	*	-		N[3:0]	U	*	_	_NW[2:	-
	Cycle Control 2	Kabii	AIII		4			_				
	Overla Control O	Daol	A OI-	*	1	0	1	0	0	0	0	1
	Cycle Control 3	R3Ch	A0h				N[3:0]				_NW[2:0	
					1	0	1	0	0	0	0	0
	Cycle Control 4	R3Dh	00h	*	*	*		I[1:0]		PI[1:0]		N[1:0]
					0	0	0	0	0	0	0	0
	Cycle Control 5	R3Eh	2Dh	*					1[7:0]			
					0	0	1	0	1	1	0	1
	Cycle Control 6	R40h	03h	*				GDO	N[7:0]			
					0	0	0	0	0	0	1	1
	Cycle Control 7	R41h	CCh	*				GDO	F[7:0]			
					1	1	0	0	1	1	0	0
Partial Image	Partial area start row 2	R0Ah	00h	*				PSL	[15:8]			
Display setting					0	0	0	0	0	0	0	0
' '	Partial area start row 1	R0Bh	00h	*					[7:0]			-
					0	0	0	0	0	0	0	0
	Partial area end row 2	R0Ch	01h	*	Ť				[15:8]			
	r artial area eria few 2	110011	0111		0	0	0	0	0	0	0	1
	Partial area end row 1	R0Dh	3Fh	*			•		.[7:0]		U	-
	Faitial alea ellu low i	RODII	31 11		0	0	1	1	1	1	1	1
Vertical Scroll	Vertical Caroll Ten	DOEL	006	*	U	U	- 1				ı	
	Vertical Scroll Top	R0Eh	00h		_	_	_	1	[15:8]		_	
setting		D0E1	0.01	*	0	0	0	0	0	0	0	0
	Vertical Scroll Top	R0Fh	00h	*					[7:0]			
	fixed area 1				0	0	0	0	0	0	0	0
	Vertical Scroll	R10h	01h	*					[15:8]			
	height area 2				0	0	0	0	0	0	0	1
	Vertical Scroll	R11h	40h	*				VSA	[7:0]			
	height area 1				0	1	0	0	0	0	0	0
	Vertical Scroll	R12h	00h	*				BFA	[15:8]			
	Button area 2				0	0	0	0	0	0	0	0
	Vertical Scroll	R13h	00h	*				BFA	[7:0]			
	Button area 1				0	0	0	0	0	0	0	0
	Vertical Scroll	R14h	00h	*				VSP	[15:8]			
	Start address 2				0	0	0	0	0	0	0	0
	Vertical Scroll	R15h	00h	*				VSF	[7:0]			
	Start address 1				0	0	0	0	0	0	0	0
Window address	Column address start 2	R02h	00h	*					15:8]			
setting			- 2		0	0	0	0	0	0	0	0
	Column address start 1	R03h	00h	*			J		[7:0]			
	Column addices stall 1	1,0011	5511		0	0	0	0	0	0	0	0
	Column address end 2	R04h	00h	*		<u> </u>	J		15:8]		3	<del></del>
	Column address end 2	110411	OUII		0	0	0			0	0	0
	Column address and 4	DOEL	EE1-	*	U	U	U	0	0	U	0	U
	Column address end 1	R05h	EFh				4	1	[7:0]	4		
	Developed to 1.0	Deel	001	*	1	1	1	0	1 1	1	1	1
	Row address start 2	R06h	00h	^		_	_		15:8]		_	
					0	0	0	0	0	0	0	0
	Row address start 1	R07h	00h	*					[7:0]		ı	,
					0	0	0	0	0	0	0	0
	Row address end 2	R08h	01h	*				EP[	15:8]			
					0	0	0	0	0	0	0	1
	Row address end 1	R09h	3Fh	*				EP	[7:0]			
					0	0	1	1	1	1	1	1
	Memory Access	R16h	08h	*	MY	MX	MV	*	BGR	*	*	*
	control				0	0	0	0	1	0	0	0
	Data control	R72h	00h	*	*	*		1[1:0]	*	*		[1:0]
			- 2		0	0	0	0	0	0	0	0
							U				0	J

Product No.	DBC-24032024-2A0	REV. 1.0	Page	19 / 32



	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Window address	Write Data	R22h					GRAN	1 Write	Data			
setting												
	wait 60 msec or more											
Display on	SAP Idle mode	R94h	0Ah	*				SAP_	_I[7:0]			
setting					0	0	0	0	1	0	1	0
	Display Control 8	R90h	7Fh	*				SAP	[7:0]			
					0	1	1	1	1	1	1	1
	Display Control 1	R26h	84h	*	PT[	1:0]	GON	DTE	D[	1:0]	*	*
					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A4h	*	PT[	1:0]	GON	DTE	D[	1:0]	*	*
					1	0	1	0	0	1	0	0
	Display Control 1	R26h	ACh	*	PT[	1:0]	GON	DTE	D[	1:0]	*	*
					1	0	1	0	1	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	BCh	*	PT	1:0]	GON	DTE	D[	1:0]	*	*
					1	0	1	1	1	1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0

# 3.5.2.2 Power OFF Sequence (Stand-by Transit Sequence)

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1
	Display Control 1	R26h	B8h	*	PT[	1:0]	GON	DTE	D[	1:0]	*	*
					1	0	1	1	1	0	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A8h	*	PT[	1:0]	GON	DTE	D[	1:0]	*	*
					1	0	1	0	1	0	0	0
	Display Control 1	R26h	84h	*	PT[	1:0]	GON	DTE	D[	1:0]	*	*
					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	80h	*		1:0]	GON	DTE		1:0]	*	*
					1	0	0	0	0	0	0	0
Power off setting	Display Control 8	R90h	00h	*					[7:0]			
					0	0	0	0	0	0	0	0
	Power Control 2	R1Ch	00h	*	*	*	*	*	*		AP[2:0]	
					0	0	0	0	0	0	0	0
	Power Control 1	R1Bh	04h	*	GAS	*	*	PON	DK	XDK	VLCD	STB
					ENB						_TRI	
				*	0	0	0	0	0	1	0	0
	VCOM Control 1	R43h	00h	*	VCOM	*	*	*	*	*	*	*
					G							
	2 2 11	D 4 D 1	0.01	*	0	0	0	0	0	0	0	0
	Power Control 1	R1Bh	0Ch	*	GAS	•	^	PON	DK	XDK	VLCD	STB
					ENB						_TRI	
TEOT4 "	TEOT4	Dool	001	*	0	0	0	0	1 0	1	0	0
TEST1 setting	TEST1	R96h	00h	Ŷ	0	0	0	0	•	0	0	0
Power off setting	Power Control 1	R1Bh	0Dh		GAS			PON	DK	XDK	VLCD	STB
					ENB	_		_	4		_TRI	
000 1 1	000 0 - 1 - 1 4	D401	001	*	0	0	0	0	1	1	0	1
OSC control	OSC Control 1	R19h	86h	,	CADJ[3:0] CUADJ[2:0				2:0]	osc_		
setting						_		_	_	4		EN
					1	0	0	0	0	1	1	0

			_		
Product No	DBC-24032024-2A0	REV/ 1.0	1	Page	20 / 32



# 3.5.2.3 Stand-by Release Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control setting	OSC Control 1	R19h	87h	*		CAD	J[3:0]		C	UADJ[2	::0]	OSC_ EN
					1	0	0	0	0	1	1	1
	wait 10 msec or more											
	Power Control 1	R1Bh	0Ch	*	GAS ENB	*	*	PON	DK	XDK	VLCD TRI	STB
					0	0	0	0	1	1	0	0
Power supply	Power Control 6	R20h	00h	*		ВТ	3:0]		*	*	*	*
setting					0	0	0	0	0	0	0	0
initializing	Power Control 5	R1Fh	07h	*	*	*	*	*		VRF	I[3:0]	
					0	0	0	0	0	1	1	1
	VCOM Control 2	R44h	7Fh	*	*			\	/CM[6:0	0]		
					0	1	1	1	1	1	1	1
	VCOM Control 3	R45h	14h	*	*	*	*			/DV[4:0		
					0	0	0	1	0	1	0	0
	Power Control 3	R1Dh	05h	*	*	*	*	*	*		VC1[2:0	
					0	0	0	0	0	1	0	1
	Power Control 4	R1Eh	00h	*	*	*	*	*	*		VC3[2:0	
					0	0	0	0	0	0	0	0
Power supply	Power Control 2	R1Ch	04h	*	*	*	*	*	*		AP[2:0]	
operation					0	0	0	0	0	1	0	0
start setting	Power Control 1	R1Bh	14h	*	GAS		*	PON	DK	XDK	VLCD	STB
					ENB						_TRI	
	: 40				0	0	0	1	0	1	0	0
	wait 40 msec or more	D 401	001	*	1/001/	*	*	*	*	*	*	*
	VCOM Control 1	R43h	80h	*	VCOM G			*			*	*
					1	0	0	0	0	0	0	0
	wait 60 msec or more											
Display on	Display Control 8	R90h	7Fh	*			1		[7:0]			
setting					0	1	1	1	1	1	1	1
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1
Display on	Display Control 1	R26h	84h	*		[1:0]	GON	DTE		1:0]	*	*
setting					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A4h	*		[1:0]	GON	DTE		1:0]	*	*
	5: 1 0 11	Door	4.01		1	0	1	0	0	1	0	0
	Display Control 1	R26h	ACh	*		[1:0]	GON	DTE		1:0]		
					1	0	1	0	1	1	0	0
	wait 40 msec or more	Dack	DO!	*	D-7	1.01	001	DTE	D.	1.01	*	*
	Display Control 1	R26h	BCh			[1:0]	GON	DTE		1:0]		
TECT1 catting	TEST1	DOCK	004	*	0	0	0	0	0	0	0	0
TEST1 setting	IESII	R96h	00h		U	U	U	U	U	U	U	U

			_		
Product No	DBC-24032024-2A0	REV/ 1.0	1	Page	21 / 32



## 3.5.2.4Refresh Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control	OSC Control 1	R19h	87h	*		CAD	J[3:0]		CI	UADJ[2	2:0]	OSC_ EN
setting					1	0	0	0	0	1	1	1
Power supply	Power Control 6	R20h	00h	*	<u> </u>	_	[3:0]		*	*	*	*
setting					0	0	0	0	0	0	0	0
initializing	Power Control 5	R1Fh	07h	*	*	*	*	*		VRH	H[3:0]	
					0	0	0	0	0	1	1	1
	VCOM Control 2	R44h	7Fh	*	*				/CM[6:0	_		
					0	1	1 *	1	1	1	1	1
	VCOM Control 3	R45h	14h	*	*					VDV[4:0		
	Power Control 3	R1Dh	05h	*	0	0	0	1 *	0	1	0	0
	Power Control 3	KIDII	บอก		0	0	0	0	0	1	VC1[2:0	<u>1</u>
	Power Control 4	R1Eh	00h	*	*	*	*	*	*		VC3[2:0	
	1 Ower Control 4	IXILII	0011		0	0	0	0	0	0	0	0
Power supply	Power Control 2	R1Ch	04h	*	*	*	*	*	*		AP[2:0]	_
operation					0	0	0	0	0	1	0	0
start setting	Power Control 1	R1Bh	14h	*	GAS ENB	*	*	PON	DK	XDK	VLCD _TRI	STB
					0	0	0	1	0	1	0	0
	VCOM Control 1	R43h	80h	*	VCOM G	*	*	*	*	*	*	*
					1	0	0	0	0	0	0	0
Power control setting	BGP Control	R42h	08h	*	*	*	*	VBGP _OE		BGF	P[3:0]	
					0	0	0	0	1	0	0	0
	Cycle Control 1	R23h	95h	*			1 -	N_DO				
	0 1 0 1 10	D041	0.51	*	1	0	0	1	0	1	0	1
	Cycle Control 2	R24h	95h		1	0	0	1	C[7:0] 0	1	0	1
	Cycle Control 3	R25h	FFh	*	<del>- '- '</del>	-	U	I_DC	_		U	
	5,0.0 00				1	1	1	1	1	1	1	1
	Power Control 7	R21h	10h	*	*	*	_	[1:0]	*	*		[1:0]
					0	0	0	1	0	0	0	0
	Power Control 11	R2Bh	00h	*	*	*	PI_PRE	E_ ESH[1:0]	E	BLANK <u></u>	_DIV[3:0	0]
					0	0	0	0	0	0	0	0
	DCCLK SYNC TO CL1	R95h	01h	*	*	*	*	*	*	*	*	DCCLK _SYNC
					0	0	0	0	0	0	0	1
OSC control setting	OSC Control 2	R1Ah	00h	*	*	*	*	*	*	*	*	OSC_ TEST
					0	0	0	0	0	0	0	0
	OSC Control 3	R93h	0Fh	*	*	*	*	*		RAD	J[3:0]	
					0	0	0	0	1	1	1	1
	Internal Use 28	R70h	66h	*	*	GS	SS	TE MODE	TEON		CSEL[2:	0]
					0	1	1	0	0	1	1	0
	Gate Scan control	R18h	01h	*	*	*	*	*	*	*	SCROL L_ON	SM
					0	0	0	0	0	0	0	1

Product No.	DBC-24032024-2A0	REV. 1.0	Page	22 / 32



	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
r control setting	r Control 1	R46h	86h	*	GSEL	(	CP1[2:0	)]	*	(	CP0[2:0	
					1	0	0	0	0	1	1	0
	r Control 2	R47h	60h	*	*	(	CN1[2:0	ון	*	(	CN0[2:0	1
					0	1	1	0	0	0	0	0
	r Control 3	R48h	01h	*	*	1	VP1[2:0	)]	*	1	VP0[2:0	
					0	0	0	0	0	0	0	1
	r Control 4	R49h	67h	*	*	1	NP3[2:0	)]	*	1	NP2[2:0	
					0	1	1	0	0	1	1	1
	r Control 5	R4Ah	46h	*	*	1	NP5[2:0	)]	*	1	NP4[2:0]	
					0	1	0	0	0	1	1	0
	r Control 6	R4Bh	13h	*	*	1	NN1[2:0	0]	*	1	NO[2:0	]
					0	0	0	1	0	0	1	1
	r Control 7	R4Ch	01h	*	*	1	NN3[2:0	)]	*	1	NN2[2:0]	]
					0	0	0	0	0	0	0	1
	r Control 8	R4Dh	67h	*	*	1	NN5[2:0	)]	*	1	NN4[2:0]	]
					0	1	1	0	0	1	1	1
	r Control 9	R4Eh	00h	*	CGMF	21[1:0]	CGM	P0[1:0]		OP0	[3:0]	
					0	0	0	0	0	0	0	0
	r Control 10	R4Fh	13h	*		CGMP2				OP1[4:0	)]	
					0	0	0	1	0	0	1	1
	r Control 11	R50h	02h	*		N1[1:0]	CGMI	N0[1:0]		ONO	[3:0]	
					0	0	0	0	0	0	1	0
	r Control 12	R51h	00h	*		CGMN2		ļ		ON1[4:0		
				*	0	0	0	0	0	0	0	0
RGB interface	RGB interface	R38h	00h	*	*	*	*	RGB_	DPL	HSPL	VSPL	EPL
control setting	control 1							EN				_
	DOD: 4 (	Dool	0.01		0	0	0	0	0	0	0	0
	RGB interface	R39h	00h		_	_		OTCLK			•	0
Diaplay central	control 2	DOZIN	026	*	0	0	0	0	0	0	0	0
Display control	Display Control 2	R27h	02h						0	N_BF	2[3:0]	0
setting	Display Control 3	R28h	03h	*	0	0	0	0	U	0 N_FF	10.510	U
	Display Control 3	112011	0311		0	0	0	0	0	0	1	1
	Display Control 4	R29h	08h	*	*	*	*	*		PI_BI	D[3·U]	'
	Display Control 4	112011	0011		0	0	0	0	1	0	0	0
	Display Control 5	R2Ah	08h	*	*	*	*	*		_	P[3:0]	
	,				0	0	0	0	1	0	0	0
	Display Control 6	R2Ch	08h	*	*	*	*	*		I BF	[3:0]	
					0	0	0	0	1	0	0	0
	Display Control 7	R2Dh	08h	*	*	*	*	*		I_FP	[3:0]	
					0	0	0	0	1	0	0	0
	Display Control 9	R35h	09h	*				EQS	[7:0]			
					0	0	0	0	1	0	0	1
	Display Control 10	R36h	09h	*					[7:0]			
					0	0	0	0	1	0	0	1
	Display Control 11	R91h	14h	*				GEN_C			_	
					0	0	0	1	0	1	0	0
	Display Control 12	R37h	00h	*	*	*		[1:0]			[3:0]	
	D: 1 M :	DC4	001		0	0	0	0	0	0	0	0
	Display Mode control	R01h	06h	*	*	*	*	*			NORON	
	Ovala Ozistisal 4	DOAL	۸ ۵ ا-	*	0	0	0	0	0 *	1 N	T NAME (	0
	Cycle Control 1	R3Ah	A1h	-	1		N[3:0]	0		0 N	_NW[2:0	
	Cycle Control 2	R3Bh	۸ <b>۱</b> ۱	*	1	DI DI	1 NI3:01	U	0		0	1
	Cycle Control 2	Kabu	A1h		1		N[3:0]	0			_NW[2:	
	Cycle Control 3	R3Ch	A0h	*	1	0 LRTI	<u>       1                             </u>	0	0 *	0	0 NW[2:0	1
	Cycle Control 3	13011	7011		1	0	1	0	0	0	_INVV[Z.U	0
	Cycle Control 4	R3Dh	00h	*	*	*		I[1:0]		PI[1:0]	DIV_N	
	Cycle Control 4	RODII	0011		0	0	0	0	0	0	0	0
					_				U	U	J	U

Product No.	DBC-24032024-2A0	REV. 1.0	Page	23 / 32



	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Display control	Cycle Control 5	R3Eh	2Dh	*		•		SON	I[7:0]			
setting					0	0	1	0	1	1	0	1
	Cycle Control 6	R40h	03h	*				GDO	N[7:0]			
					0	0	0	0	0	0	1	1
	Cycle Control 7	R41h	CCh	*				GDO	F[7:0]			
					1	1	0	0	1	1	0	0
Patial Image	Partial area start row 2	R0Ah	00h	*				PSL	[15:8]			
Display setting					0	0	0	0	0	0	0	0
	Partial area start row 1	R0Bh	00h	*				PSL	[7:0]			
					0	0	0	0	0	0	0	0
	Partial area end row 2	R0Ch	01h	*					[15:8]			
					0	0	0	0	0	0	0	1
	Partial area end row 1	R0Dh	3Fh	*					[7:0]			
					0	0	1	1	1	1	1	1
Vertical Scroll	Vertical Scroll Top	R0Eh	00h	*		_			15:8]		_	_
setting					0	0	0	0	0	0	0	0
	Vertical Scroll Top	R0Fh	00h	*					[7:0]	_	_	
	fixed area 1	DAOL	041-	*	0	0	0	0	0	0	0	0
	Vertical Scroll	R10h	01h	_ ^	_	0			[15:8]	^	^	4
	height area 2	DAAL	401	+	0	0	0	0	0	0	0	1
	Vertical Scroll	R11h	40h		_	1	_		[7:0]	_	0	_
	height area 1 Vertical Scroll	R12h	00h	*	0	1	0	0 DEAI	0	0	U	0
	Button area 2	K IZN	oon		0	0	0	0	[15:8] 0	0	0	0
	Vertical Scroll	R13h	00h	*	U	U	U	_	[7:0]	U	U	U
	Button area 1	KISII	UUII		0	0	0	0	0	0	0	0
	Vertical Scroll	R14h	00h	*	-	U	U	_	[15:8]	U	U	U
	Start address 2	171411	0011		0	0	0	0	0	0	0	0
	Vertical Scroll	R15h	00h	*					[7:0]		U	U
	Start address 1	111011	0011		0	0	0	0	0	0	0	0
Window address	Column address start 2	R02h	00h	*	- ŭ		Ū		15:8]	J	J	J
setting					0	0	0	0	0	0	0	0
	Column address start 1	R03h	00h	*				SC	7:0]	_		
					0	0	0	0	0	0	0	0
	Column address end 2	R04h	00h	*				ECI.	15:8]		I.	
					0	0	0	0	0	0	0	0
	Column address end 1	R05h	EFh	*				EC	[7:0]			
					1	1	1	0	1	1	1	1
	Row address start 2	R06h	00h	*				SP[	15:8]			
					0	0	0	0	0	0	0	0
	Row address start 1	R07h	00h	*					7:0]			
					0	0	0	0	0	0	0	0
	Row address end 2	R08h	01h	*	_	-	-		15:8]	-	_	
					0	0	0	0	0	0	0	1
	Row address end 1	R09h	3Fh	*			1		7:0]		T	
		<b>5</b> ( 5 )	0.51		0	0	1	1	1	1	1	1
	Memory Access	R16h	08h	*	MY	MX	MV	*	BGR	*	*	*
	control	D.7.0.	0.01	,	0 *	0	0	0	1 *	0	0	0
	Data control	R72h	00h	*		*		[1:0]				[1:0]
Diamlay	CADId	DC4!	0.4.1	*	0	0	0	0	0	0	0	0
Display on	SAP Idle mode	R94h	0Ah	_ ^					<u>[[7:0]</u>	_		_
setting		DOOL	70-	*	0	0	0	0	1 1	0	1	0
	Display Control 8	R90h	7Fh		_	4	4		[7:0]	4	4	4
	Display Control 1	Dock	DC <sub>b</sub>	*	0	1	1 CON	DTE	1	1	1	1
	Display Control 1	R26h	BCh		1 1	[1:0] 0	GON 1	1	1	1:0] 1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0
TEST I Setting	ILOII	1/9011	UUII		U	U	U	U	U	U	U	U

			_		
Product No.	DBC-24032024-2A0	REV. 1.0		Page	24 / 32



## **4 OPTICAL SPECIFICATION**

### 4.1 OPTICAL CHARACTERISTICS

Measuring instruments: CS1000 (KONICA MINOLTA), LCD7000 (OTSUKA ELECTRONICS)

EZcontrast160D (ELDIM)

Driving condition: VCI = IOVCC = 2.7V, VSS = 0V

Optimized VCOMDC

VLCD= | Vsigpp±Vcompp | /2

Backlight: IL=10mA Measured temperature:  $Ta = 25^{\circ} C$ 

Ta = 25 °C

Item Symbol		Condition	MIN	TYP	MAX	Unit	Note No.	Note	
Response Time	Rise Time	TON	VLCD=0.7V→5.0V	-	-	40	ms	1	*
Resp	Fall Time	TOFF	VLCD=5.0V→0.7V	-	-	60	ms	'	
Contrast Ratio	Backlight ON	CR	VI CD 0.7V/5.0V	240	400	-			
Conf	Backlight OFF	CR	VLCD=0.7V/5.0V	-	8.5	-		2	
_	Left	θL		80	-	-	deg		
Viewing Angle	Right	θR	VLCD= 0.7V/5.0V	80	-	1	deg	3	*
/iewing	Up	Øυ	0.7 V/3.0 V CR ≥ 10	80	-	ı	deg		
	Down	ØD		80	-	-	deg		
		V90		1.3	1.6	1.9	V		
V-T T	Threshold Voltage V50			1.8	2.1	2.4	V	4	*
		V10		2.4	2.7	3.0	V		
White	e V-T Curve			Refer to Curve	Fig. 3 : W	hite V-T			Reference
White	e Chromaticity	х у	VLCD= 0.7V	Fig. 4: \ Range	White Chro	maticity		5	
Burn-in			No noticeable burn-in image should be observed after 2hours of window pattern display.		bserved		6		
Centre Brightness		VLCD= 0.7V	210	300	-	cd/m <sup>2</sup>	7		
Brigh	tness Distribution		VLCD= 0.7V	70	-	-	%	8	

<sup>\*</sup> Measured in the form of LCD module

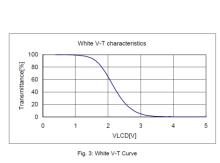
.

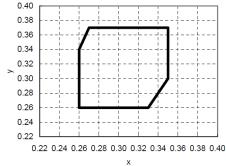
			_		
Product No.	DBC-24032024-2A0	REV. 1.0		Page	25 / 32



### 4.1.1 Test Method

Note	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white.  White Black White White 100% 90% 10% 10% 10% 10% 10% 10% 10% 10% 10% 1	LCD7000	Black display VLCD=5.0V White display VLCD=0.7V TON Rise Time TOFF Fall Time
2	Contrast ratio	Measure maximum luminance Y1 (VLCD=0.7V) and minimum luminance Y2 (VLCD=5.0V) at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2  Diameter of measuring point: 8mm Ø	CS1000 LCD7000	Backlight ON Backlight OFF
3	Viewing angle Horizontal θ Vertical Ø	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10	EZcontrast160D	
4	V-T Threshold Value	Change VLCD by 0.1V step and plot the points where the luminance is 90% as V90, 50% as V50 and 10% as V10 of maximum luminance.  100% 90% 50% 10% V90 V50 V10	LCD7000	
5	White chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system at VLCD=0.7V Colour matching faction: 2° view	CS1000	
6	Burn-in	Visually check burn-in image on the screen after 2 hours of "window display" (VLCD=0.7V/5.0V).		At optimized VCOMDC
7	Centre brightness	Measure the brightness at the centre of the screen	CS1000	
8	Brightness distribution	(Brightness distribution)= 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points	CS1000	





[White Chromaticity Range]

X	У
0.27	0.37
0.26	0.34
0.26	0.26
0.33	0.26
0.35	0.30
0.35	0.37

Product No.	DBC-24032024-2A0	REV. 1.0
-------------	------------------	----------

Page 26 / 32



### **5 BACKLIGHT SPECIFICATION**

#### 5.1 LED DRIVING CONDITIONS

Item	Symbol	Condition		Rating	Unit	Applicable		
item	Gyillboi	Condition	Min	Тур	Max	Oille	Terminal	
Forward Current	IL25	Ta=25 °C	-	10	35	mA		
Forward Current	IL70	Ta= 70°C	-	-	15	mA	BLH-BLL	
Forward Voltage	VL	Ta= 25°C, IL= 10mA	-	6.0	6.5	V		
Estimated Life of LED	LL	Ta= 25°C, IL= 10mA Note	-	(50,000)	-	hr		

#### Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
  The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

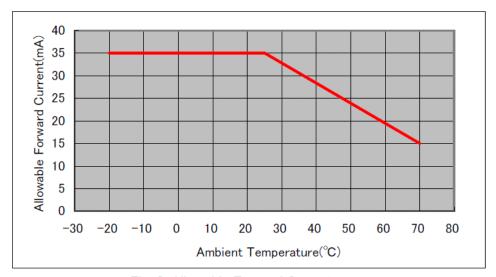
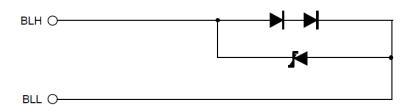


Fig. 2: Allowable Forward Current

#### 5.2 LED CIRCUIT



Product No. DBC-24032024-2A0 REV. 1.0	Page 27 / 32	
---------------------------------------	--------------	--



### **6 QUALITY ASSURANCE SPECIFICATION**

### 6.1 DEFECTIVE DISPLAY AND SCREEN QUALITY

Observed TFT-LCD monitor from front during operation with the following conditions

Driving signal Raster Pattern (RGB in monochrome, white black)

Signal condition VLCD: 0.7V, 2.1 V, 5.0V (3 Steps)

Observation Distance 30cm

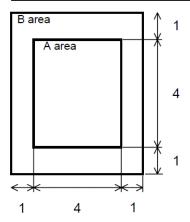
Illuminance 200 to 350 lx Backlight IL= 10mA

De	fect item		Defect content	Criteria		
	Line defect	Black, white or color	r line, 3 or more neighboring defective dots	Not exists		
Display Quality	Dot defect	TFT or CF, or dust is (brighter dot, darker High bright dot: Visil Low bright dot: Visil	on dot-by-dot base due to defective s counted as dot defect dot) ble through 2% ND filter at VLCD=5.0V ble through 5% ND filter at VLCD=5.0V ark through white display at VLCD=2.1V	Refer to table 1		
	Dirt	Point-like uneven br	ightness (white stain, black stain etc)	Invisible through 1% ND filter		
ı₹			0.25mm< <i>ϕ</i>	N=0		
Quality	Foreign	Point-like	0.20< <i>φ</i> ≦0.25mm	N≦2		
	particle		$\phi \leq$ 0.20mm	Ignored		
en	particle	Liner	3.0mm <length 0.08mm<width<="" and="" td=""><td>N=0</td></length>	N=0		
<u>e</u>			length≦3.0mm or width≦0.08mm	Ignored		
S	Diner Liner  Others			Use boundary sample for judgment when necessary		

φ(mm): Average diameter = (major axis + minor axis)/2 Permissible number: N

#### Table 1

Table					
Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
Α	0	2	2		Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more
В	2	4	4		Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
Total	2	4	4	5	



Division of A and B areas B area: Active area

Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

Product No.	DBC-24032024-2A0	REV. 1.0	
-------------	------------------	----------	--



## 6.2 SCREEN AND OTHER APPEARANCE

Testing conditions

Illuminance 1200~2000 lx

Observation distance 30cm

	Item	Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only
	S-case	No functional defect occurs	
	FPC cable	No functional defect occurs	

Page	29	/ 32



#### 6.3 DEALING WITH CUSTOMER COMPLAINTS

#### 6.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

#### 6.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

Product No.	DBC-24032024-2A0	REV. 1.0		Page	30 / 32	l
-------------	------------------	----------	--	------	---------	---

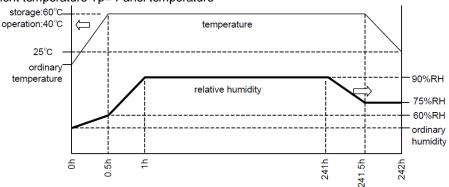


## **7 RELIABILITY SPECIFICATION**

## 7.1 RELIABILITY TESTS

Test Item		Test Condition	Number of failures/ number of examinations	
Durability Test	High Temperature Storage	Ta= 80°C 240h	0/3	
	Low Temperature Storage	Ta=-30°C 240h	0/3	
	High Temperature & High Humidity Storage	Ta= 60°C, RH= 90% Non condensing 240h	0/3	
	High Temperature Operation	Tp= 70°C 240h	0/3	
ural	Low Temperature Operation	Tp= -20°C 240h	0/3	
۵	High Temperature & Humidity Operation	Tp= 40°C RH= 90% 240h Non condensing	0/3	
	Thermal Shock Storage	-30←→ 80°C (30 min/ 30min) 100cycles	0/3	
Test	Electrostatic Discharge Test (non operation)	Confirms to EIAJ ED-4701/300 C= 200 pF, R= 0 $\Omega$ , V= $\pm 200$ V Each 3 times of discharge on and power supply and other terminals.	0/3	
Mechanical Environmental Test	Surface Discharge Test (non operation)	C= 250 pF, R= 100 Ω, V=± 12kV Each 5 times of discharge in both polarities on the centre of screen with the case and Touch Panel terminal grounded.	0/3	
ical E	Vibration test	Total amplitude 1.5 mm, f= 10~55 Hz, X,Y,Z directions for each 2 hours.	0/3	
Mechani	Impact test	Use original jig and make an impact with peak acceleration of 1000 m/s²for 6 ms with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-1995	0/3	
Packing Test	Packing Vibration-Proof Test	Acceleration of 19.6 m/s <sup>2</sup> with frequency of 10 → 55 → 10 Hz, X, Y, Z direction for each 30 minutes.	0/1 Packing	
	Packing Drop Test	Drop from 75 cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	0/1 Packing	





Reliability Criteria: measure following parameters after leaving the TFT at 25°C for 2 hours or more.

Item	Standard	Remark
Display quality	No visible abnormalities shall be seen	As per Quality Assurance Specification
Contrast ratio	40 or more	Backlight ON

Product No. DBC-24032024-2A0	REV. 1.0	ļ	Page	31 / 32	
------------------------------	----------	---	------	---------	--



#### 8 HANDLING PRECAUTIONS

#### Safety

If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.

If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

#### Mounting and Design

Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.

When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.

Design the system so that no input signal is given unless the power supply voltage is applied.

#### Caution during LCD cleaning

Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.

Do not wipe the display surface with dry or hard materials that will damage the polariser surface.

Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

#### Caution against static charge

As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS. Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

#### **Packaging**

Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height.

To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

#### Caution during operation

It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

#### Storage

Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH. Store the display in a clean environment, free from dust, organic solvents and corrosive gases.

Do not crash, shake or jolt the display (including accessories).

Product No. DBC-24032024-2A0 REV. 1.0	Page 32 / 32	<u> </u>
---------------------------------------	--------------	----------