LIQUID CRYSTAL DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**
CUSTOMER PART NUMBER	
PRODUCT NUMBER	**DBC-24032024-2A0**

Product Mgr	Design Eng
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Date: 11-Jul-12	Date: 11-Jul-12

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECN no.
1.0	11-Jul-12			First Issue	

1 MAIN FEATURES

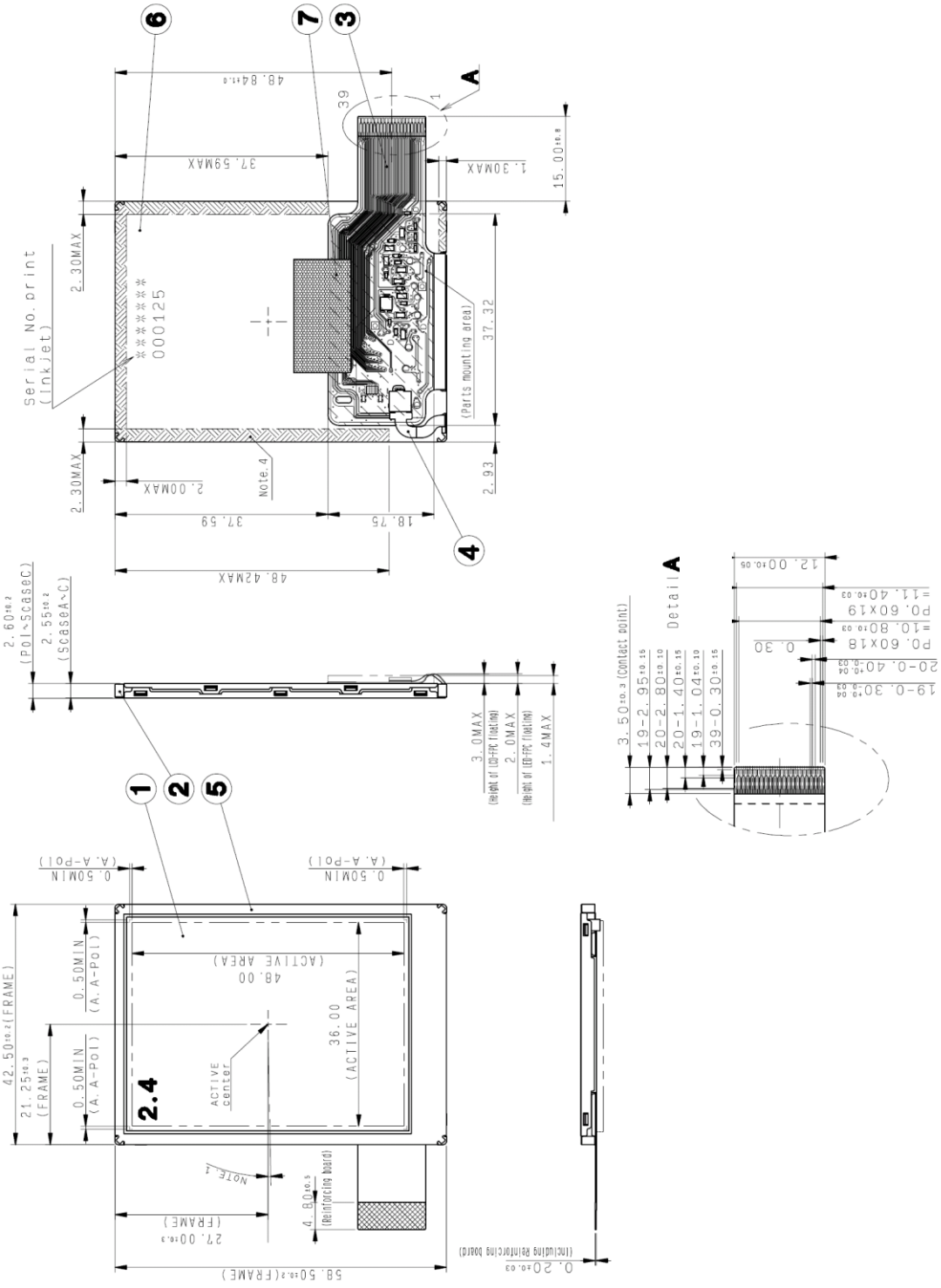
ITEM	CONTENTS
Screen Size	2.4” Diagonal
Display Format	240 x RGB x 320 Dots
N° of Colour	262k
Overall Dimensions	42.50 mm (H) x 58.50 mm (V) x 2.60 mm (D)
Active Area	36.00 mm (H) x 48.00 mm (V)
LCD Type	TFT
Mode	Sunlight Readable
Interface	CPU 16 / 18-bit
Backlight Type	LED
Operating Temperature	-20°C ~ +70°C
Storage Temperature	-30°C ~ +80°C
RoHS compliant	Yes

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	240 x RGB x 320	Dots
Overall Dimensions	42.50 mm (H) x 58.50 mm (V) x 2.60 mm (D)	mm
Bezel Opening Area	-	mm
Active Area	36.00 mm (H) x 48.00 mm (V)	mm
Dot Pitch	50.0 (H) x RGB x 150.0 (V)	µm
Weight	13.6	g

2.2 MECHANICAL DRAWING



Note 1. Angular deviation of LCD cell from the TFT-LCD monitor's reference axis shall be less than ±40°.
Note 2. Recommended FPC connectors. For LCD: HIROSE, part number: FH23-39S-0.3SHW(05)
Note 3. Protective film is affixed on front surface of the screen. Location tolerance of the protective film shall be ±1.5 mm to the polarising film.
Note 4. In case TFT-LCD monitor is fixed to the case of your product, it is recommended that monitor is fixed to area.
Note 5. Refer to "QUALITY ASSURANCE SPECIFICATION" about the appearance specification of a polarizer.

1. LCD
2. Frame
3. LCD-FPC
4. LED-FPC
5. S-Case A
6. S-Case C
7. I - Tape

2.3 SERIAL LABEL / PRINT

The label / print indicates the least significant digit of manufacture year (1digit), manufacture month with below alphabet (1letter), model code (4 or 5 characters), serial number (6 digits).

* Label / Print Contents

*	*	****(*)	******
a	b	c	d

where:

a The least significant digit of manufacturing year

b Manufacturing Month:
Jan-A, Feb-B, Mar-C, Apr-D, May-E, Jun-F, Jul-G, Aug-H, Sep-I, Oct-J, Nov-K, Dec-L

c Model code
24AJC →Made in Japan
24AKC →Made in Malaysia
24ALC →Made in China

d Serial number, like “000125”

Examples:

Made in Japan
0K24AJC000125
means "manufactured in November 2010, model 24AJC, serial number 000125"

Made in Malaysia
0K24AKC000125
means "manufactured in November 2010, model 24AKC, serial number 000125"

Made in China
0K24ALC000125
means "manufactured in November 2010, model 24ALC, serial number 000125"

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Condition	Min	Max	Unit	Applicable terminal
Supply Voltage	VCI	Ta=25˚C	-0.3	4.6	V	VCI
Supply Voltage for Logic	IOVCC		-0.3	VCI	V	IOVCC
Input Voltage for Logic	VI		-0.3	IOVCC+0.3	V	RESETB, CSB, RS, WRB, DO-D17, BSO, BS1, RDB

3.2 ELECTRICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable terminal
Supply Voltage	VCI	Ta=25˚C	2.6	2.7	3.6	V	VCI
Supply Voltage for Logic	IOVCC		1.65	VCI	VCI	V	IOVCC
Input Voltage for Logic	VI		0	-	IOVCC	V	RESETB, CSB, RS, WRB, DO-D17, BSO, BS1, RDB
Input Voltage for Logic	VIH		0.7xIOVCC	-	IOVCC	V	RESETB, CSB, RS, WRB, DO-D17, BSO, BS1, RDB
	VIL		0	-	0.3xIOVCC		
Output Voltage for Logic	VOH	IOH=0.1mA	0.8xIOVCC	-	-	V	DO-D17, TE
	VOL	IOL=0.1mA	-	-	0.2xIOVCC	V	
Operating Current	ICI	Colour bar display, still image	-	5.5	11.0	mA	VCI
	IOICC		-	0.5	1.0	µA	IOVCC
Standby Current	ICIs	Other input with constant voltage	-	1.0	2.0	µA	VCI
	IOICCs		-	6.0	25.0	µA	IOVCC

Note: a still image (colour bar) on display, when CPU does not access the GRAM.

3.3 INTERFACE PIN ASSIGNMENT

3.3.1 LCM PIN ASSIGNMENT

Pin No.	Symbol	Function
1	VSS	Ground
2	VSS	Ground
3	VCI	Power supply
4	IOVCC	Power supply
5	VSS	Ground
6	RESETB	Reset signal. When RESETB is Lo, an internal reset is performed
7	CSB	Chip select signal (Active Low)
8	RS	Select register signal (Lo: index; Hi: command or display data)
9	WRB	Write strobe signal
10	VSS	Ground
11	D0	Data Bus
12	D1	Data Bus
13	D2	Data Bus
14	D3	Data Bus
15	D4	Data Bus
16	D5	Data Bus
17	D6	Data Bus
18	D7	Data Bus
19	D8	Data Bus
20	D9	Data Bus
21	D10	Data Bus
22	D11	Data Bus
23	D12	Data Bus
24	D13	Data Bus
25	D14	Data Bus
26	D15	Data Bus
27	D16	Data Bus (connect it to VSS when using 16-bit interface)
28	D17	Data Bus (connect it to VSS when using 16-bit interface)
29	VSS	Ground
30	BS0	Interface mode selection
31	BS1	Interface mode selection
32	RDB	Read strobe signal (connect it to IOVCC when not used)
33	NC	Open
34	NC	Open
35	NC	Open
36	NC	Open
37	TE	Frame head output pulse (connect it to IOVCC when not used)
38	BLH	LED drive power source (Anode side)
39	BLL	LED drive power source (Cathode side)

Recommended connector: Hirose Electric FH23 series [FH23-39S-0.3SHW(05)]
As FCB cable has gold plated terminals, gilt finish contact shoe connector is recommended.

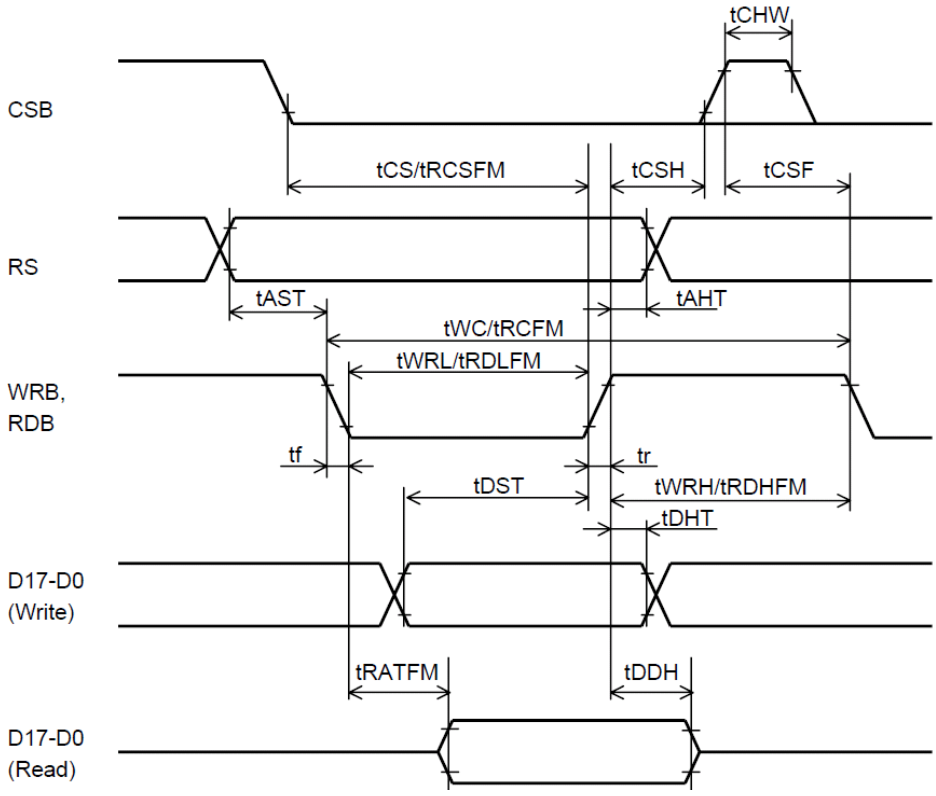
3.4 TIMING CHARACTERISTICS

3.4.1 AC Timing Characteristics

Unless otherwise noted, Ta=25°C, VCI=IOVCC=2.7V, VSS=0V

Item	Symbol	Condition	Rating		Unit
			MIN	MAX	
Address setup time	tAST	RS	10	-	ns
Address hold time	that	RS	10	-	ns
CSB high level pulse width	tCHW	CSB	0	-	ns
CSB setup time	tCS	CSB-WRB	35	-	ns
	tRCSFM	CSB-WRB	180	-	
CSB wait time	tCSF	CSB	10	-	ns
CSB hold time	tCSH	CSB	10	-	ns
WRB bus cycle time	tWC	WRB	100	-	ns
WRB high level pulse width	tWRH	WRB	15	-	ns
WRB low level pulse width	tWRL	WRB	20	-	ns
RDB bus cycle time	tRCFM	WRB	250	-	ns
RDB high level pulse width	tRDHFM	WRB	15	-	ns
RDB low level pulse width	tRDLFM	WRB	180	-	ns
WRB data setup time	tDST	D17-D0	10	-	ns
WRB data hold time	tDHT	D17-D0	10	-	ns
RDB access time	tRATFM	D17-D0	-	340	ns
RDB output disable time	tDDH	D17-D0	20	80	ns
Input signal rising time	tr	-	-	15	ns
Input signal falling time	tf	-	-	15	ns

The switching voltage is set at 30% to 70% of IOVCC voltage



3.5 INTERFACE

Bus Width	Index/ Command Write	GRAM Write			
		CPU			
		18bit	16bit	16bit	8bit
Transferring Method		18	16	16+2	6+6+6
Width of data of 1 pixel		18	16	18	18
BS1	*	H	L	L	H
BS0	*	L	L	H	H

D17			R5					
D16			R4					
D15			R3	R5/R0	R5			
D14			R2	R4	R4			
D13			R1	R3	R3			
D12			R0	R2	R2			
D11			G5	R1	R1			
D10			G4	G5	R0			
D9			G3	G4	G5			
D8			G2	G3	G4			
D7	ID7	RB7	G1	G2	G3	R5	G5	B5
D6	ID6	RB6	G0	G1	G2	R4	G4	B4
D5	ID5	RB5	B5	G0	G1	R3	G3	B3
D4	ID4	RB4	B4	B5/B0	G0	R2	G2	B2
D3	ID3	RB3	B3	B4	B5	R1	G1	B1
D2	ID2	RB2	B2	B3	B4	R0	G0	B0
D1	ID1	RB1	B1	B2	B3	B1		
D0	ID0	RB0	B0	B1	B2	B0		

Please connect any unused terminal of D0-D17 to VSS

3.5.1 REGISTER LIST

Register			D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R01h	Display Mode control		*	*	*	*	*	IDMON	INVON	NORON	PTLON
	initial	(0006h)						0	1	1	0
	recommend	(0006h)						0	1	1	0
R02h	Column address start 2		*	SC[15:8]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R03h	Column address start 1		*	SC[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R04h	Column address end 2		*	EC[15:8]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R05h	Column address end 1		*	EC[7:0]							
	initial	(00EFh)		1	1	1	0	1	1	1	1
	recommend	(00EFh)		1	1	1	0	1	1	1	1
R06h	Row address start 2		*	SP[15:8]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R07h	Row address start 1		*	SP[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R08h	Row address end 2		*	EP[15:8]							
	initial	(0001h)		0	0	0	0	0	0	0	1
	recommend	(0001h)		0	0	0	0	0	0	0	1
R09h	Row address end 1		*	EP[7:0]							
	initial	(003Fh)		0	0	1	1	1	1	1	1
	recommend	(003Fh)		0	0	1	1	1	1	1	1
R0Ah	Partial area start row 2		*	PSL[15:8]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R0Bh	Partial area start row 1		*	PSL[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R0Ch	Partial area end row 2		*	PEL[15:8]							
	initial	(0001h)		0	0	0	0	0	0	0	1
	recommend	(0001h)		0	0	0	0	0	0	0	1
R0Dh	Partial area end row 1		*	PEL[7:0]							
	initial	(003Fh)		0	0	1	1	1	1	1	1
	recommend	(003Fh)		0	0	1	1	1	1	1	1
R0Eh	Vertical Scroll Top fixed area 2		*	TFA[15:8]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R0Fh	Vertical Scroll Top fixed area 1		*	TFA[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R10h	Vertical Scroll height area 2		*	VSA[15:8]							
	initial	(0001h)		0	0	0	0	0	0	0	1
	recommend	(0001h)		0	0	0	0	0	0	0	1
R11h	Vertical Scroll height area 1		*	VSA[7:0]							
	initial	(0040h)		0	1	0	0	0	0	0	0
	recommend	(0040h)		0	1	0	0	0	0	0	0
R12h	Vertical Scroll Button area 2		*	BFA[15:8]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0

Register			D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R13h	Vertical Scroll Button area 1		*	BFA[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R14h	Vertical Scroll Start address 2		*	VSP[15:8]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R15h	Vertical Scroll Start address 1		*	VSP[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R16h	Memory Access control		*	MY	MX	MV	*	BGR	*	*	*
	initial	(0000h)		0	0	0		0			
	recommend	(0008h)		0	0	0		1			
R18h	Gate Scan control		*	*	*	*	*	*	*	SCROLL_ON	SM
	initial	(0000h)								0	0
	recommend	(0001h)								0	1
R19h	OSC Control 1		*	CADJ[3:0]				CUADJ[2:0]			OSC_EN
	initial	(0086h)		1	0	0	0	0	1	1	0
	recommend	(0087h)		1	0	0	0	0	1	1	1
R1Ah	OSC Control 2		*	*	*	*	*	*	*	*	OSC_TEST
	initial	(0000h)									0
	recommend	(0000h)									0
R1Bh	Power Control 1		*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
	initial	(0000h)		0			0	0	0	0	0
	recommend	(0014h)		0			1	0	1	0	0
R1Ch	Power Control 2		*	*	*	*	*	*	AP[2:0]		
	initial	(0004h)							1	0	0
	recommend	(0004h)							1	0	0
R1Dh	Power Control 3		*	*	*	*	*	*	VC1[2:0]		
	initial	(0004h)							1	0	0
	recommend	(0005h)							1	0	1
R1Eh	Power Control 4		*	*	*	*	*	*	VC3[2:0]		
	initial	(0000h)							0	0	0
	recommend	(0000h)							0	0	0
R1Fh	Power Control 5		*	*	*	*	*	VRH[3:0]			
	initial	(0006h)						0	1	1	0
	recommend	(0007h)						0	1	1	1
R20h	Power Control 6		*	BT[3:0]				*	*	*	*
	initial	(0060h)		0	1	1	0				
	recommend	(0000h)		0	0	0	0				
R21h	Power Control 7		*	*	*	FS1[1:0]		*	*	FS0[1:0]	
	initial	(0010h)				0	1			0	0
	recommend	(0010h)				0	1			0	0
R22h	Write Data		GRAM Write								
	initial	(0000h)									
	recommend	(0000h)									
R23h	Cycle Control 1		*	N_DC[7:0]							
	initial	(0095h)		1	0	0	1	0	1	0	1
	recommend	(0095h)		1	0	0	1	0	1	0	1
R24h	Cycle Control 2		*	PI_DC[7:0]							
	initial	(0095h)		1	0	0	1	0	1	0	1
	recommend	(0095h)		1	0	0	1	0	1	0	1

Register			D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R25h	Cycle Control 3		*	I_DC[7:0]							
	initial	(00FFh)		1	1	1	1	1	1	1	1
	recommend	(00FFh)		1	1	1	1	1	1	1	1
R26h	Display Control 1		*	PT[1:0]		GON	DTE	D[1:0]		*	*
	initial	(00A0h)		1	0	1	0	0	0		
	recommend	(00BCh)		1	0	1	1	1	1		
R27h	Display Control 2		*	*	*	*	*	N_BP[3:0]			
	initial	(0002h)						0	0	1	0
	recommend	(0002h)						0	0	1	0
R28h	Display Control 3		*	*	*	*	*	N_FP[3:0]			
	initial	(0002h)						0	0	1	0
	recommend	(0003h)						0	0	1	1
R29h	Display Control 4		*	*	*	*	*	PI_BP[3:0]			
	initial	(0002h)						0	0	1	0
	recommend	(0008h)						1	0	0	0
R2Ah	Display Control 5		*	*	*	*	*	PI_FP[3:0]			
	initial	(0002h)						0	0	1	0
	recommend	(0008h)						1	0	0	0
R2Bh	Power Control 11		*	*	*	PI_PRE_ REFRESH[1:0]		BLANK_DIV[3:0]			
	initial	(0000h)				0	0	0	0	0	0
	recommend	(0000h)				0	0	0	0	0	0
R2Ch	Display Control 6		*	*	*	*	*	I_BP[3:0]			
	initial	(0002h)						0	0	1	0
	recommend	(0008h)						1	0	0	0
R2Dh	Display Control 7		*	*	*	*	*	I_FP[3:0]			
	initial	(0002h)						0	0	1	0
	recommend	(0008h)						1	0	0	0
R35h	Display Control 9		*	EQS[7:0]							
	initial	(0009h)		0	0	0	0	1	0	0	1
	recommend	(0009h)		0	0	0	0	1	0	0	1
R36h	Display Control 10		*	EQP[7:0]							
	initial	(0009h)		0	0	0	0	1	0	0	1
	recommend	(0009h)		0	0	0	0	1	0	0	1
R37h	Display Control 12		*	*	*	PTG[1:0]		ISC[3:0]			
	initial	(0000h)				0	0	0	0	0	0
	recommend	(0000h)				0	0	0	0	0	0
R38h	RGB interface control 1		*	*	*	*	RGB_ EN	DPL	HSPL	VSPL	EPL
	initial	(0000h)					0	0	0	0	0
	recommend	(0000h)					0	0	0	0	0
R39h	RGB interface control 2		*	DOTCLK_DIV[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R3Ah	Cycle Control 1		*	N_RTN[3:0]				*	N_NW[2:0]		
	initial	(0001h)		0	0	0	0		0	0	1
	recommend	(00A1h)		1	0	1	0		0	0	1
R3Bh	Cycle Control 2		*	PI_RTN[3:0]				*	PI_NW[2:0]		
	initial	(0001h)		0	0	0	0		0	0	1
	recommend	(00A1h)		1	0	1	0		0	0	1
R3Ch	Cycle Control 3		*	I_RTN[3:0]				*	I_NW[2:0]		
	initial	(00F0h)		1	1	1	1		0	0	0
	recommend	(00A0h)		1	0	1	0		0	0	0

Register			D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R3Dh	Cycle Control 4		*	*	*	DIV_I[1:0]		DIV_PI[1:0]		DIV_N[1:0]	
	initial	(0000h)				0	0	0	0	0	0
	recommend	(0000h)				0	0	0	0	0	0
R3Eh	Cycle Control 5		*	SON[7:0]							
	initial	(0038h)		0	0	1	1	1	0	0	0
	recommend	(002Dh)		0	0	1	0	1	1	0	1
R40h	Cycle Control 6		*	GDON[7:0]							
	initial	(0003h)		0	0	0	0	0	0	1	1
	recommend	(0003h)		0	0	0	0	0	0	1	1
R41h	Cycle Control 7		*	GDOF[7:0]							
	initial	(00F8h)		1	1	1	1	1	0	0	0
	recommend	(00CCh)		1	1	0	0	1	1	0	0
R42h	BGP Control		*	*	*	*	VBGP_OE	BGP[3:0]			
	initial	(0008h)					0	1	0	0	0
	recommend	(0008h)					0	1	0	0	0
R43h	VCOM Control 1		*	VCOMG	*	*	*	*	*	*	*
	initial	(0080h)		1							
	recommend	(0080h)		1							
R44h	VCOM Control 2		*	*	VCM[6:0]						
	initial	(005Ah)			1	0	1	1	0	1	0
	recommend	(007Fh)			1	1	1	1	1	1	1
R45h	VCOM Control 3		*	*	*	*	VDV[4:0]				
	initial	(0011h)					1	0	0	0	1
	recommend	(0014h)					1	0	1	0	0
R46h	r Control 1		*	GSEL	CP1[2:0]			*	CP0[2:0]		
	initial	(0000h)		0	0	0	0		0	0	0
	recommend	(0086h)		1	0	0	0		1	1	0
R47h	r Control 2		*	*	CN1[2:0]			*	CN0[2:0]		
	initial	(0000h)			0	0	0		0	0	0
	recommend	(0060h)			1	1	0		0	0	0
R48h	r Control 3		*	*	NP1[2:0]			*	NP0[2:0]		
	initial	(0000h)			0	0	0		0	0	0
	recommend	(0001h)			0	0	0		0	0	1
R49h	r Control 4		*	*	NP3[2:0]			*	NP2[2:0]		
	initial	(0000h)			0	0	0		0	0	0
	recommend	(0067h)			1	1	0		1	1	1
R4Ah	r Control 5		*	*	NP5[2:0]			*	NP4[2:0]		
	initial	(0000h)			0	0	0		0	0	0
	recommend	(0046h)			1	0	0		1	1	0
R4Bh	r Control 6		*	*	NN1[2:0]			*	NN0[2:0]		
	initial	(0000h)			0	0	0		0	0	0
	recommend	(0013h)			0	0	1		0	1	1
R4Ch	r Control 7		*	*	NN3[2:0]			*	NN2[2:0]		
	initial	(0000h)			0	0	0		0	0	0
	recommend	(0001h)			0	0	0		0	0	1
R4Dh	r Control 8		*	*	NN5[2:0]			*	NN4[2:0]		
	initial	(0000h)			0	0	0		0	0	0
	recommend	(0067h)			1	1	0		1	1	1
R4Eh	r Control 9		*	CGMP1[1:0]		CGMP0[1:0]		OP0[3:0]			
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0

Register			D17-8	D7	D6	D5	D4	D3	D2	D1	D0
R4Fh	r Control 10		*	CGMP3	CGMP2	*	OP1[4:0]				
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0013h)		0	0	0	1	0	0	1	1
R50h	r Control 11		*	CGMN1[1:0]		CGMN0[1:0]		ON0[3:0]			
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0002h)		0	0	0	0	0	0	1	0
R51h	r Control 12		*	CGMN3	CGMN2	*	ON1[4:0]				
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R52h	OTP Control 1		*	OTP_MASK[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R53h	OTP Control 2		*	OTP_INDEX[7:0]							
	initial	(00FFh)		1	1	1	1	1	1	1	1
	recommend	(00FFh)		1	1	1	1	1	1	1	1
R54h	OTP Control 3		*	OTP_LOAD_DISABLE	DCCLK_DISABLE	OTP_POR	OTP_PWE	OTP_PTM	0	VPP_SEL	OTP_PROG
	initial	(0008h)		0	0	0	0	1		0	0
	recommend	(0008h)		0	0	0	0	1		0	0
R64h	Internal Use 16		*	ID1[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R65h	Internal Use 17		*	*	ID2[6:0]						
	initial	(0000h)			0	0	0	0	0	0	0
	recommend	(0000h)			0	0	0	0	0	0	0
R66h	Internal Use 18		*	ID3[7:0]							
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0
R67h	Internal Use 19		*	ID4[7:0]							
	initial	(0047h)		0	1	0	0	0	1	1	1
	recommend	(0047h)		0	1	0	0	0	1	1	1
R70h	Internal Use 28		*	*	GS	SS	TE MODE	TEON	CSEL[2:0]		
	initial	(0006h)			0	0	0	0	1	1	0
	recommend	(0066h)			1	1	0	0	1	1	0
R72h	Data control		*	*	*	DFM[1:0]		*	*	TRI[1:0]	
	initial	(0000h)				0	0			0	0
	recommend	(0000h)				0	0			0	0
R90h	Display Control 8		*	SAP[7:0]							
	initial	(000Ah)		0	0	0	0	1	0	1	0
	recommend	(007Fh)		0	1	1	1	1	1	1	1
R91h	Display Control 11		*	GEN_OFF[7:0]							
	initial	(0014h)		0	0	0	1	0	1	0	0
	recommend	(0014h)		0	0	0	1	0	1	0	0
R93h	OSC Control 3		*	*	*	*	*	RADJ[3:0]			
	initial	(000Fh)						1	1	1	1
	recommend	(000Fh)						1	1	1	1
R94h	SAP Idle mode		*	SAP_I[7:0]							
	initial	(000Ah)		0	0	0	0	1	0	1	0
	recommend	(000Ah)		0	0	0	0	1	0	1	0
R95h	DCCLK SYNC TO CL1		*	*	*	*	*	*	*	*	DCCLK_SYNC
	initial	(0000h)									0
	recommend	(0001h)									1
R96h	TEST1		*	*	*	*	*	*	*	*	TEST1
	initial	(0000h)		0	0	0	0	0	0	0	0
	recommend	(0000h)		0	0	0	0	0	0	0	0

3.5.2 SEQUENCE

3.5.2.1Power ON Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
	RESETB=1											
	wait 1 msec or more											
	RESETB=0											
	wait 10 usec or more											
	RESETB=1											
	wait 120 msec or more											
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1
OSC control setting	OSC Control 1	R19h	87h	*	CADJ[3:0]				CUADJ[2:0]			OSC_EN
					1	0	0	0	0	1	1	1
	wait 10 msec or more											
Display OFF setting	Display Control 1	R26h	80h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	0	0	0
	Power Control 1	R1Bh	0Ch	*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	0	1	1	0	0
	VCOM Control 1	R43h	00h	*	VCOMG	*	*	*	*	*	*	*
					0	0	0	0	0	0	0	0
Power supply setting initializing	Power Control 6	R20h	00h	*	BT[3:0]				*	*	*	*
					0	0	0	0	0	0	0	0
	Power Control 5	R1Fh	07h	*	*	*	*	*	VRH[3:0]			
					0	0	0	0	0	1	1	1
	VCOM Control 2	R44h	7Fh	*	*	VCM[6:0]						
					0	1	1	1	1	1	1	1
	VCOM Control 3	R45h	14h	*	*	*	*	VDV[4:0]				
					0	0	0	1	0	1	0	0
	Power Control 3	R1Dh	05h	*	*	*	*	*	*	VC1[2:0]		
					0	0	0	0	0	1	0	1
	Power Control 4	R1Eh	00h	*	*	*	*	*	*	VC3[2:0]		
					0	0	0	0	0	0	0	0
Power supply operation start setting	Power Control 2	R1Ch	04h	*	*	*	*	*	*	AP[2:0]		
					0	0	0	0	0	1	0	0
	Power Control 1	R1Bh	14h	*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	1	0	1	0	0
	wait 40 msec or more											
	VCOM Control 1	R43h	80h	*	VCOMG	*	*	*	*	*	*	*
					1	0	0	0	0	0	0	0
Power control setting	BGP Control	R42h	08h	*	*	*	*	VBGP_OE	BGP[3:0]			
					0	0	0	0	1	0	0	0
	Cycle Control 1	R23h	95h	*	N_DC[7:0]							
					1	0	0	1	0	1	0	1
	Cycle Control 2	R24h	95h	*	PI_DC[7:0]							
					1	0	0	1	0	1	0	1
	Cycle Control 3	R25h	FFh	*	I_DC[7:0]							
					1	1	1	1	1	1	1	1
	Power Control 7	R21h	10h	*	*	*	FS1[1:0]		*	*	FS0[1:0]	
					0	0	0	1	0	0	0	0
	Power Control 11	R2Bh	00h	*	*	*	PI_PRE_REFRESH[1:0]		BLANK_DIV[3:0]			
					0	0	0	0	0	0	0	0
	DCCLK SYNC TO CL1	R95h	01h	*	*	*	*	*	*	*	*	DCCLK_SYNC
					0	0	0	0	0	0	0	1

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control setting	OSC Control 2	R1Ah	00h	*	*	*	*	*	*	*	*	OSC_TEST
					0	0	0	0	0	0	0	0
	OSC Control 3	R93h	0Fh	*	*	*	*	*	RADJ[3:0]			
					0	0	0	0	1	1	1	1
	Internal Use 28	R70h	66h	*	*	GS	SS	TE MODE	TEON	CSEL[2:0]		
					0	1	1	0	0	1	1	0
	Gate Scan control	R18h	01h	*	*	*	*	*	*	*	SCROL L_ON	SM
					0	0	0	0	0	0	0	1
r control setting	r Control 1	R46h	86h	*	GSEL	CP1[2:0]			*	CP0[2:0]		
					1	0	0	0	0	1	1	0
	r Control 2	R47h	60h	*	*	CN1[2:0]			*	CN0[2:0]		
					0	1	1	0	0	0	0	0
	r Control 3	R48h	01h	*	*	NP1[2:0]			*	NP0[2:0]		
					0	0	0	0	0	0	0	1
	r Control 4	R49h	67h	*	*	NP3[2:0]			*	NP2[2:0]		
					0	1	1	0	0	1	1	1
	r Control 5	R4Ah	46h	*	*	NP5[2:0]			*	NP4[2:0]		
					0	1	0	0	0	1	1	0
	r Control 6	R4Bh	13h	*	*	NN1[2:0]			*	NN0[2:0]		
					0	0	0	1	0	0	1	1
	r Control 7	R4Ch	01h	*	*	NN3[2:0]			*	NN2[2:0]		
					0	0	0	0	0	0	0	1
	r Control 8	R4Dh	67h	*	*	NN5[2:0]			*	NN4[2:0]		
					0	1	1	0	0	1	1	1
	r Control 9	R4Eh	00h	*	CGMP1[1:0]		CGMP0[1:0]		OP0[3:0]			
					0	0	0	0	0	0	0	0
	r Control 10	R4Fh	13h	*	CGMP3	CGMP2	*	OP1[4:0]				
					0	0	0	1	0	0	1	1
	r Control 11	R50h	02h	*	CGMN1[1:0]		CGMN0[1:0]		ON0[3:0]			
					0	0	0	0	0	0	1	0
	r Control 12	R51h	00h	*	CGMN3	CGMN2	*	ON1[4:0]				
					0	0	0	0	0	0	0	0
RGB interface control setting	RGB interface control 1	R38h	00h	*	*	*	*	RGB_ EN	DPL	HSPL	VSPL	EPL
					0	0	0	0	0	0	0	0
	RGB interface control 2	R39h	00h	*	DOTCLK_DIV[7:0]							
					0	0	0	0	0	0	0	0
Display control setting	Display Control 2	R27h	02h	*	*	*	*	*	N_BP[3:0]			
					0	0	0	0	0	0	1	0
	Display Control 3	R28h	03h	*	*	*	*	*	N_FP[3:0]			
					0	0	0	0	0	0	1	1
	Display Control 4	R29h	08h	*	*	*	*	*	PI_BP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 5	R2Ah	08h	*	*	*	*	*	PI_FP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 6	R2Ch	08h	*	*	*	*	*	I_BP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 7	R2Dh	08h	*	*	*	*	*	I_FP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 9	R35h	09h	*	EQS[7:0]							
					0	0	0	0	1	0	0	1
	Display Control 10	R36h	09h	*	EQP[7:0]							
					0	0	0	0	1	0	0	1
	Display Control 11	R91h	14h	*	GEN_OFF[7:0]							
					0	0	0	1	0	1	0	0
	Display Control 12	R37h	00h	*	*	*	PTG[1:0]		ISC[3:0]			
					0	0	0	0	0	0	0	0

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Display control setting	Display Mode control	R01h	06h	*	*	*	*	*	IDMON	INVON	NORON	PTLON
					0	0	0	0	0	1	1	0
	Cycle Control 1	R3Ah	A1h	*	N_RTN[3:0]				*	N_NW[2:0]		
					1	0	1	0	0	0	0	1
	Cycle Control 2	R3Bh	A1h	*	PI_RTN[3:0]				*	PI_NW[2:0]		
					1	0	1	0	0	0	0	1
	Cycle Control 3	R3Ch	A0h	*	I_RTN[3:0]				*	I_NW[2:0]		
					1	0	1	0	0	0	0	0
	Cycle Control 4	R3Dh	00h	*	*	*	DIV_I[1:0]		DIV_PI[1:0]		DIV_N[1:0]	
					0	0	0	0	0	0	0	0
	Cycle Control 5	R3Eh	2Dh	*	SON[7:0]							
					0	0	1	0	1	1	0	1
	Cycle Control 6	R40h	03h	*	GDON[7:0]							
					0	0	0	0	0	0	1	1
	Cycle Control 7	R41h	CCh	*	GDOF[7:0]							
					1	1	0	0	1	1	0	0
Partial Image Display setting	Partial area start row 2	R0Ah	00h	*	PSL[15:8]							
					0	0	0	0	0	0	0	0
	Partial area start row 1	R0Bh	00h	*	PSL[7:0]							
					0	0	0	0	0	0	0	0
	Partial area end row 2	R0Ch	01h	*	PEL[15:8]							
					0	0	0	0	0	0	0	1
	Partial area end row 1	R0Dh	3Fh	*	PEL[7:0]							
					0	0	1	1	1	1	1	1
Vertical Scroll setting	Vertical Scroll Top fixed area 2	R0Eh	00h	*	TFA[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Top fixed area 1	R0Fh	00h	*	TFA[7:0]							
					0	0	0	0	0	0	0	0
	Vertical Scroll height area 2	R10h	01h	*	VSA[15:8]							
					0	0	0	0	0	0	0	1
	Vertical Scroll height area 1	R11h	40h	*	VSA[7:0]							
					0	1	0	0	0	0	0	0
	Vertical Scroll Button area 2	R12h	00h	*	BFA[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Button area 1	R13h	00h	*	BFA[7:0]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Start address 2	R14h	00h	*	VSP[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Start address 1	R15h	00h	*	VSP[7:0]							
					0	0	0	0	0	0	0	0
Window address setting	Column address start 2	R02h	00h	*	SC[15:8]							
					0	0	0	0	0	0	0	0
	Column address start 1	R03h	00h	*	SC[7:0]							
					0	0	0	0	0	0	0	0
	Column address end 2	R04h	00h	*	EC[15:8]							
					0	0	0	0	0	0	0	0
	Column address end 1	R05h	EFh	*	EC[7:0]							
					1	1	1	0	1	1	1	1
	Row address start 2	R06h	00h	*	SP[15:8]							
					0	0	0	0	0	0	0	0
	Row address start 1	R07h	00h	*	SP[7:0]							
					0	0	0	0	0	0	0	0
	Row address end 2	R08h	01h	*	EP[15:8]							
					0	0	0	0	0	0	0	1
	Row address end 1	R09h	3Fh	*	EP[7:0]							
					0	0	1	1	1	1	1	1
	Memory Access control	R16h	08h	*	MY	MX	MV	*	BGR	*	*	*
					0	0	0	0	1	0	0	0
	Data control	R72h	00h	*	*	*	DFM[1:0]		*	*	TRI[1:0]	
					0	0	0	0	0	0	0	0

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Window address setting	Write Data	R22h		GRAM Write Data								
	wait 60 msec or more											
Display on setting	SAP Idle mode	R94h	0Ah	*	SAP_I[7:0]							
					0	0	0	0	1	0	1	0
	Display Control 8	R90h	7Fh	*	SAP[7:0]							
					0	1	1	1	1	1	1	1
	Display Control 1	R26h	84h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A4h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	0	0	1	0	0
	Display Control 1	R26h	ACh	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	0	1	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	BCh	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	1	1	1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0

3.5.2.2Power OFF Sequence (Stand-by Transit Sequence)

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1
	Display Control 1	R26h	B8h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	1	1	0	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A8h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	0	1	0	0	0
	Display Control 1	R26h	84h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	80h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	0	0	0
Power off setting	Display Control 8	R90h	00h	*	SAP[7:0]							
					0	0	0	0	0	0	0	0
	Power Control 2	R1Ch	00h	*	*	*	*	*	*	AP[2:0]		
					0	0	0	0	0	0	0	0
	Power Control 1	R1Bh	04h	*	GAS ENB	*	*	PON	DK	XDK	VLCD _TRI	STB
					0	0	0	0	0	1	0	0
	VCOM Control 1	R43h	00h	*	VCOM G	*	*	*	*	*	*	*
					0	0	0	0	0	0	0	0
	Power Control 1	R1Bh	0Ch	*	GAS ENB	*	*	PON	DK	XDK	VLCD _TRI	STB
					0	0	0	0	1	1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0
Power off setting	Power Control 1	R1Bh	0Dh	*	GAS ENB	*	*	PON	DK	XDK	VLCD _TRI	STB
					0	0	0	0	1	1	0	1
OSC control setting	OSC Control 1	R19h	86h	*	CADJ[3:0]				CUADJ[2:0]			OSC_ EN
					1	0	0	0	0	1	1	0

3.5.2.3 Stand-by Release Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control setting	OSC Control 1	R19h	87h	*	CADJ[3:0]				CUADJ[2:0]			OSC_EN
					1	0	0	0	0	1	1	1
	wait 10 msec or more											
	Power Control 1	R1Bh	0Ch	*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	0	1	1	0	0
Power supply setting initializing	Power Control 6	R20h	00h	*	BT[3:0]				*	*	*	*
					0	0	0	0	0	0	0	0
	Power Control 5	R1Fh	07h	*	*	*	*	*	VRH[3:0]			
					0	0	0	0	0	1	1	1
	VCOM Control 2	R44h	7Fh	*	*	VCM[6:0]						
					0	1	1	1	1	1	1	1
	VCOM Control 3	R45h	14h	*	*	*	*	VDV[4:0]				
					0	0	0	1	0	1	0	0
	Power Control 3	R1Dh	05h	*	*	*	*	*	*	VC1[2:0]		
					0	0	0	0	0	1	0	1
	Power Control 4	R1Eh	00h	*	*	*	*	*	*	VC3[2:0]		
					0	0	0	0	0	0	0	0
Power supply operation start setting	Power Control 2	R1Ch	04h	*	*	*	*	*	*	AP[2:0]		
					0	0	0	0	0	1	0	0
	Power Control 1	R1Bh	14h	*	GAS ENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	1	0	1	0	0
	wait 40 msec or more											
	VCOM Control 1	R43h	80h	*	VCOMG	*	*	*	*	*	*	*
					1	0	0	0	0	0	0	0
	wait 60 msec or more											
Display on setting	Display Control 8	R90h	7Fh	*	SAP[7:0]							
					0	1	1	1	1	1	1	1
TEST1 setting	TEST1	R96h	01h	*	0	0	0	0	0	0	0	1
Display on setting	Display Control 1	R26h	84h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	0	0	0	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	A4h	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	0	0	1	0	0
	Display Control 1	R26h	ACh	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	0	1	1	0	0
	wait 40 msec or more											
	Display Control 1	R26h	BCh	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	1	1	1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0

3.5.2.4Refresh Sequence

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
OSC control setting	OSC Control 1	R19h	87h	*	CADJ[3:0]				CUADJ[2:0]			OSC_EN
					1	0	0	0	0	1	1	1
Power supply setting initializing	Power Control 6	R20h	00h	*	BT[3:0]				*	*	*	*
					0	0	0	0	0	0	0	0
	Power Control 5	R1Fh	07h	*	*	*	*	*	VRH[3:0]			
					0	0	0	0	0	1	1	1
	VCOM Control 2	R44h	7Fh	*	*	VCM[6:0]						
					0	1	1	1	1	1	1	1
	VCOM Control 3	R45h	14h	*	*	*	*	VDV[4:0]				
					0	0	0	1	0	1	0	0
	Power Control 3	R1Dh	05h	*	*	*	*	*	*	VC1[2:0]		
					0	0	0	0	0	1	0	1
	Power Control 4	R1Eh	00h	*	*	*	*	*	*	VC3[2:0]		
					0	0	0	0	0	0	0	0
Power supply operation start setting	Power Control 2	R1Ch	04h	*	*	*	*	*	*	AP[2:0]		
					0	0	0	0	0	1	0	0
	Power Control 1	R1Bh	14h	*	GASENB	*	*	PON	DK	XDK	VLCD_TRI	STB
					0	0	0	1	0	1	0	0
	VCOM Control 1	R43h	80h	*	VCOMG	*	*	*	*	*	*	*
					1	0	0	0	0	0	0	0
Power control setting	BGP Control	R42h	08h	*	*	*	*	VBGP_OE	BGP[3:0]			
					0	0	0	0	1	0	0	0
	Cycle Control 1	R23h	95h	*	N_DC[7:0]							
					1	0	0	1	0	1	0	1
	Cycle Control 2	R24h	95h	*	PI_DC[7:0]							
					1	0	0	1	0	1	0	1
	Cycle Control 3	R25h	FFh	*	I_DC[7:0]							
					1	1	1	1	1	1	1	1
	Power Control 7	R21h	10h	*	*	*	FS1[1:0]		*	*	FS0[1:0]	
					0	0	0	1	0	0	0	0
	Power Control 11	R2Bh	00h	*	*	*	PI_PRE_REFRESH[1:0]		BLANK_DIV[3:0]			
					0	0	0	0	0	0	0	0
	DCCLK SYNC TO CL1	R95h	01h	*	*	*	*	*	*	*	*	DCCLK_SYNC
					0	0	0	0	0	0	0	1
OSC control setting	OSC Control 2	R1Ah	00h	*	*	*	*	*	*	*	*	OSC_TEST
					0	0	0	0	0	0	0	0
	OSC Control 3	R93h	0Fh	*	*	*	*	*	RADJ[3:0]			
					0	0	0	0	1	1	1	1
	Internal Use 28	R70h	66h	*	*	GS	SS	TE MODE	TEON	CSEL[2:0]		
					0	1	1	0	0	1	1	0
	Gate Scan control	R18h	01h	*	*	*	*	*	*	*	SCROL_ON	SM
					0	0	0	0	0	0	0	1

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
r control setting	r Control 1	R46h	86h	*	GSEL	CP1[2:0]			*	CP0[2:0]		
					1	0	0	0	0	1	1	0
	r Control 2	R47h	60h	*	*	CN1[2:0]			*	CN0[2:0]		
					0	1	1	0	0	0	0	0
	r Control 3	R48h	01h	*	*	NP1[2:0]			*	NP0[2:0]		
					0	0	0	0	0	0	0	1
	r Control 4	R49h	67h	*	*	NP3[2:0]			*	NP2[2:0]		
					0	1	1	0	0	1	1	1
	r Control 5	R4Ah	46h	*	*	NP5[2:0]			*	NP4[2:0]		
					0	1	0	0	0	1	1	0
	r Control 6	R4Bh	13h	*	*	NN1[2:0]			*	NN0[2:0]		
					0	0	0	1	0	0	1	1
	r Control 7	R4Ch	01h	*	*	NN3[2:0]			*	NN2[2:0]		
					0	0	0	0	0	0	0	1
	r Control 8	R4Dh	67h	*	*	NN5[2:0]			*	NN4[2:0]		
					0	1	1	0	0	1	1	1
	r Control 9	R4Eh	00h	*	CGMP1[1:0]		CGMP0[1:0]		OP0[3:0]			
					0	0	0	0	0	0	0	0
	r Control 10	R4Fh	13h	*	CGMP3	CGMP2	*		OP1[4:0]			
					0	0	0	1	0	0	1	1
	r Control 11	R50h	02h	*	CGMN1[1:0]		CGMN0[1:0]		ON0[3:0]			
					0	0	0	0	0	0	1	0
	r Control 12	R51h	00h	*	CGMN3	CGMN2	*		ON1[4:0]			
					0	0	0	0	0	0	0	0
RGB interface control setting	RGB interface control 1	R38h	00h	*	*	*	*	RGB_EN	DPL	HSPL	VSPL	EPL
					0	0	0	0	0	0	0	0
	RGB interface control 2	R39h	00h	*	DOTCLK_DIV[7:0]							
					0	0	0	0	0	0	0	0
Display control setting	Display Control 2	R27h	02h	*	*	*	*	*	N_BP[3:0]			
					0	0	0	0	0	0	1	0
	Display Control 3	R28h	03h	*	*	*	*	*	N_FP[3:0]			
					0	0	0	0	0	0	1	1
	Display Control 4	R29h	08h	*	*	*	*	*	PI_BP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 5	R2Ah	08h	*	*	*	*	*	PI_FP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 6	R2Ch	08h	*	*	*	*	*	I_BP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 7	R2Dh	08h	*	*	*	*	*	I_FP[3:0]			
					0	0	0	0	1	0	0	0
	Display Control 9	R35h	09h	*	EQS[7:0]							
					0	0	0	0	1	0	0	1
	Display Control 10	R36h	09h	*	EQP[7:0]							
					0	0	0	0	1	0	0	1
	Display Control 11	R91h	14h	*	GEN_OFF[7:0]							
					0	0	0	1	0	1	0	0
	Display Control 12	R37h	00h	*	*	*	PTG[1:0]		ISC[3:0]			
					0	0	0	0	0	0	0	0
	Display Mode control	R01h	06h	*	*	*	*	*	IDMON	INVON	NORON	PTLON
					0	0	0	0	0	1	1	0
	Cycle Control 1	R3Ah	A1h	*	N_RTN[3:0]				*	N_NW[2:0]		
					1	0	1	0	0	0	0	1
	Cycle Control 2	R3Bh	A1h	*	PI_RTN[3:0]				*	PI_NW[2:0]		
					1	0	1	0	0	0	0	1
	Cycle Control 3	R3Ch	A0h	*	I_RTN[3:0]				*	I_NW[2:0]		
					1	0	1	0	0	0	0	0
	Cycle Control 4	R3Dh	00h	*	*	*	DIV_I[1:0]		DIV_PI[1:0]		DIV_N[1:0]	
					0	0	0	0	0	0	0	0

	Function	Register	Recom	D17-8	D7	D6	D5	D4	D3	D2	D1	D0
Display control setting	Cycle Control 5	R3Eh	2Dh	*	SON[7:0]							
					0	0	1	0	1	1	0	1
	Cycle Control 6	R40h	03h	*	GDON[7:0]							
					0	0	0	0	0	0	1	1
	Cycle Control 7	R41h	CCh	*	GDOF[7:0]							
					1	1	0	0	1	1	0	0
Patial Image Display setting	Partial area start row 2	R0Ah	00h	*	PSL[15:8]							
					0	0	0	0	0	0	0	0
	Partial area start row 1	R0Bh	00h	*	PSL[7:0]							
					0	0	0	0	0	0	0	0
	Partial area end row 2	R0Ch	01h	*	PEL[15:8]							
					0	0	0	0	0	0	0	1
	Partial area end row 1	R0Dh	3Fh	*	PEL[7:0]							
					0	0	1	1	1	1	1	1
Vertical Scroll setting	Vertical Scroll Top fixed area 2	R0Eh	00h	*	TFA[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Top fixed area 1	R0Fh	00h	*	TFA[7:0]							
					0	0	0	0	0	0	0	0
	Vertical Scroll height area 2	R10h	01h	*	VSA[15:8]							
					0	0	0	0	0	0	0	1
	Vertical Scroll height area 1	R11h	40h	*	VSA[7:0]							
					0	1	0	0	0	0	0	0
	Vertical Scroll Button area 2	R12h	00h	*	BFA[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Button area 1	R13h	00h	*	BFA[7:0]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Start address 2	R14h	00h	*	VSP[15:8]							
					0	0	0	0	0	0	0	0
	Vertical Scroll Start address 1	R15h	00h	*	VSP[7:0]							
					0	0	0	0	0	0	0	0
Window address setting	Column address start 2	R02h	00h	*	SC[15:8]							
					0	0	0	0	0	0	0	0
	Column address start 1	R03h	00h	*	SC[7:0]							
					0	0	0	0	0	0	0	0
	Column address end 2	R04h	00h	*	EC[15:8]							
					0	0	0	0	0	0	0	0
	Column address end 1	R05h	EFh	*	EC[7:0]							
					1	1	1	0	1	1	1	1
	Row address start 2	R06h	00h	*	SP[15:8]							
					0	0	0	0	0	0	0	0
	Row address start 1	R07h	00h	*	SP[7:0]							
					0	0	0	0	0	0	0	0
	Row address end 2	R08h	01h	*	EP[15:8]							
					0	0	0	0	0	0	0	1
	Row address end 1	R09h	3Fh	*	EP[7:0]							
					0	0	1	1	1	1	1	1
	Memory Access control	R16h	08h	*	MY	MX	MV	*	BGR	*	*	*
					0	0	0	0	1	0	0	0
	Data control	R72h	00h	*	*	*	DFM[1:0]		*	*	TRI[1:0]	
					0	0	0	0	0	0	0	0
Display on setting	SAP Idle mode	R94h	0Ah	*	SAP_I[7:0]							
					0	0	0	0	1	0	1	0
	Display Control 8	R90h	7Fh	*	SAP[7:0]							
					0	1	1	1	1	1	1	1
	Display Control 1	R26h	BCh	*	PT[1:0]		GON	DTE	D[1:0]		*	*
					1	0	1	1	1	1	0	0
TEST1 setting	TEST1	R96h	00h	*	0	0	0	0	0	0	0	0

4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Measuring instruments: CS1000（KONICA MINOLTA), LCD7000 (OTSUKA ELECTRONICS)
EZcontrast160D（ELDIM)
Driving condition: VCI = IOVCC = 2.7V, VSS = 0V
Optimized VCOMDC
VLCD=｜Vsigpp±Vcompp｜/2
Backlight: IL=10mA
Measured temperature: Ta ＝ 25° C

Ta = 25 °C

Item		Symbol	Condition	MIN	TYP	MAX	Unit	Note No.	Note
Response Time	Rise Time	TON	VLCD=0.7V→5.0V	-	-	40	ms	1	*
	Fall Time	TOFF	VLCD=5.0V→0.7V	-	-	60	ms		
Contrast Ratio	Backlight ON	CR	VLCD=0.7V/5.0V	240	400	-		2	
	Backlight OFF			-	8.5	-			
Viewing Angle	Left	θL	VLCD= 0.7V/5.0V CR ≥ 10	80	-	-	deg	3	*
	Right	θR		80	-	-	deg		
	Up	ØU		80	-	-	deg		
	Down	ØD		80	-	-	deg		
V-T Threshold Voltage		V90		1.3	1.6	1.9	V	4	*
		V50		1.8	2.1	2.4	V		
		V10		2.4	2.7	3.0	V		
White V-T Curve				Refer to Fig. 3 : White V-T Curve					Reference
White Chromaticity		x	VLCD= 0.7V	Fig. 4: White Chromaticity Range				5	
		y							
Burn-in				No noticeable burn-in image should be observed after 2hours of window pattern display.				6	
Centre Brightness			VLCD= 0.7V	210	300	-	cd/m²	7	
Brightness Distribution			VLCD= 0.7V	70	-	-	%	8	

* Measured in the form of LCD module

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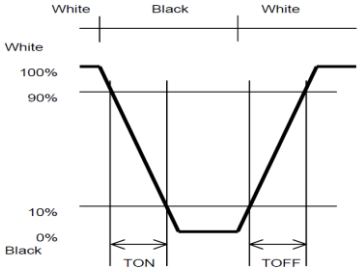
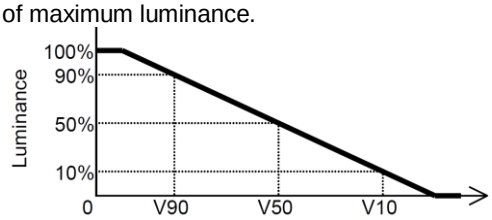
4.1.1 Test Method

Note	Item	Test method	Measuring instrument	Remark
1	Response time	Measure output signal waveform by the luminance meter when raster of window pattern is changed from white to black and from black to white. 	LCD7000	Black display VLCD=5.0V White display VLCD=0.7V TON Rise Time TOFF Fall Time
2	Contrast ratio	Measure maximum luminance Y1 (VLCD=0.7V) and minimum luminance Y2 (VLCD=5.0V) at the centre of the screen by displaying raster or window pattern. Then calculate the ratio between these two values. Contrast ratio = Y1/Y2 Diameter of measuring point: 8mm Ø	CS1000 LCD7000	Backlight ON Backlight OFF
3	Viewing angle Horizontal θ Vertical Ø	Move the luminance meter from right to left and up and down and determinate the angles where contrast ratio is 10	EZcontrast160D	
4	V-T Threshold Value	Change VLCD by 0.1V step and plot the points where the luminance is 90% as V90, 50% as V50 and 10% as V10 of maximum luminance. 	LCD7000	
5	White chromaticity	Measure chromaticity coordinates x and y of CIE1931 colorimetric system at VLCD=0.7V Colour matching faction: 2° view	CS1000	
6	Burn-in	Visually check burn-in image on the screen after 2 hours of “window display” (VLCD=0.7V/5.0V).		At optimized VCOMDC
7	Centre brightness	Measure the brightness at the centre of the screen	CS1000	
8	Brightness distribution	(Brightness distribution)= 100 x B/A % A: max. brightness of the 9 points B: min. brightness of the 9 points	CS1000	

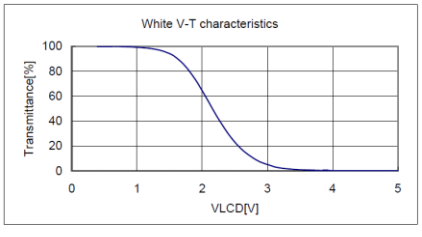
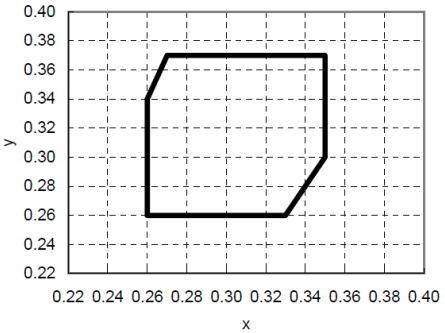


Fig. 3: White V-T Curve



【White Chromaticity Range】

x	y
0.27	0.37
0.26	0.34
0.26	0.26
0.33	0.26
0.35	0.30
0.35	0.37

5 BACKLIGHT SPECIFICATION

5.1 LED DRIVING CONDITIONS

Item	Symbol	Condition	Rating			Unit	Applicable Terminal
			Min	Typ	Max		
Forward Current	IL25	Ta=25 °C	-	10	35	mA	BLH-BLL
	IL70	Ta= 70°C	-	-	15	mA	
Forward Voltage	VL	Ta= 25°C, IL= 10mA	-	6.0	6.5	V	
Estimated Life of LED	LL	Ta= 25°C, IL= 10mA Note	-	(50,000)	-	hr	

Note:

- The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not a guarantee.
- This figure is estimated for an LED operating alone.
  The performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

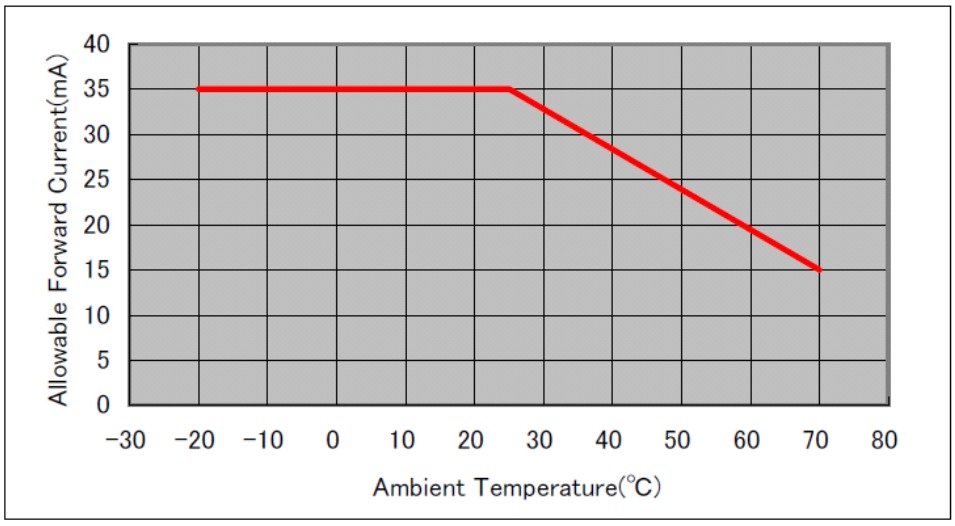
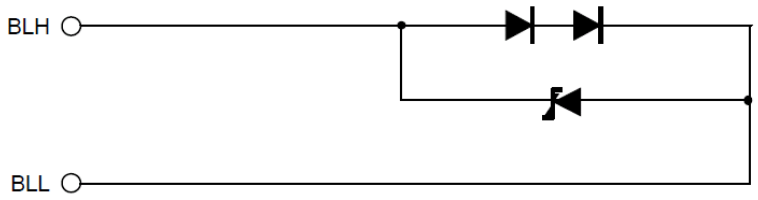


Fig. 2: Allowable Forward Current

5.2 LED CIRCUIT



6 QUALITY ASSURANCE SPECIFICATION

6.1 DEFECTIVE DISPLAY AND SCREEN QUALITY

Observed TFT-LCD monitor from front during operation with the following conditions

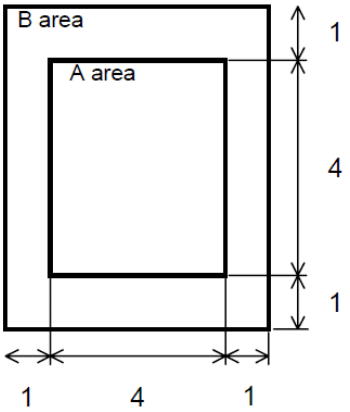
Driving signal	Raster Pattern (RGB in monochrome, white black)
Signal condition	VLCD: 0.7V, 2.1 V, 5.0V (3 Steps)
Observation Distance	30cm
Illuminance	200 to 350 lx
Backlight	IL= 10mA

Defect item		Defect content		Criteria
Display Quality	Line defect	Black, white or color line, 3 or more neighboring defective dots		Not exists
	Dot defect	Uneven brightness on dot-by-dot base due to defective TFT or CF, or dust is counted as dot defect (brighter dot, darker dot) High bright dot: Visible through 2% ND filter at VLCD=5.0V Low bright dot: Visible through 5% ND filter at VLCD=5.0V Dark dot: Appear dark through white display at VLCD=2.1V		Refer to table 1
Screen Quality	Dirt	Point-like uneven brightness (white stain, black stain etc)		Invisible through 1% ND filter
	Foreign particle	Point-like	0.25mm< ϕ	N=0
			0.20< ϕ ≦0.25mm	N≦2
			ϕ ≦0.20mm	Ignored
		Liner	3.0mm<length and 0.08mm<width	N=0
			length≦3.0mm or width≦0.08mm	Ignored
	Others			Use boundary sample for judgment when necessary

φ(mm): Average diameter = (major axis + minor axis)/2
Permissible number: N

Table 1

Area	High bright dot	Low bright dot	Dark dot	Total	Criteria
A	0	2	2	3	Permissible distance between same color bright dots (includes neighboring dots): 3 mm or more Permissible distance between same color high bright dots (includes neighboring dots): 5 mm or more
B	2	4	4	5	
Total	2	4	4	5	



Division of A and B areas
B area: Active area
Dimensional ratio between A and B areas: 1: 4: 1 (Refer to the left figure)

6.2 SCREEN AND OTHER APPEARANCE

Testing conditions
Illuminance 1200~2000 lx
Observation distance 30cm

Item		Criteria	Remark
Polarizer	Flaw Stain Bubble Dust Dent	Ignore invisible defect when the backlight is on.	Applicable area: Active area only
S-case		No functional defect occurs	
FPC cable		No functional defect occurs	

6.3 DEALING WITH CUSTOMER COMPLAINTS

6.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample. After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

6.3.2 Handling of non-conforming displays

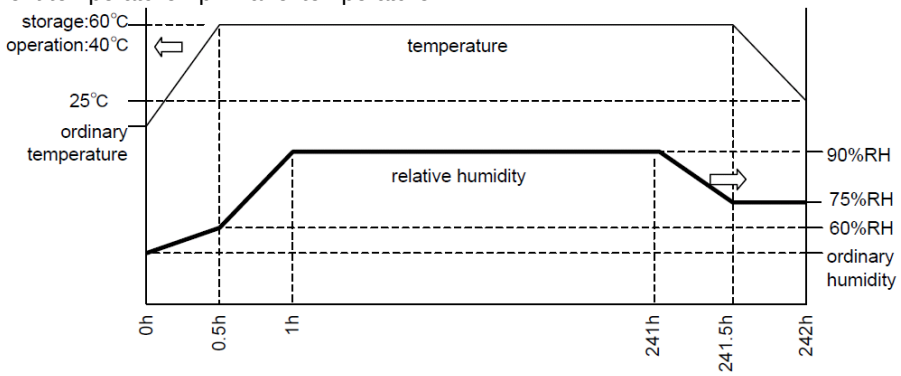
If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7 RELIABILITY SPECIFICATION

7.1 RELIABILITY TESTS

Test Item		Test Condition	Number of failures/ number of examinations
Durability Test	High Temperature Storage	Ta= 80˚C 240h	0/3
	Low Temperature Storage	Ta=-30˚C 240h	0/3
	High Temperature & High Humidity Storage	Ta= 60°C, RH= 90% Non condensing 240h	0/3
	High Temperature Operation	Tp= 70°C 240h	0/3
	Low Temperature Operation	Tp= -20°C 240h	0/3
	High Temperature & Humidity Operation	Tp= 40°C RH= 90% 240h Non condensing	0/3
	Thermal Shock Storage	-30←→ 80°C (30 min/ 30min) 100cycles	0/3
Mechanical Environmental Test	Electrostatic Discharge Test (non operation)	Confirms to EIAJ ED-4701/300 C= 200 pF, R= 0 Ω, V= ±200V Each 3 times of discharge on and power supply and other terminals.	0/3
	Surface Discharge Test (non operation)	C= 250 pF, R= 100 Ω, V=± 12kV Each 5 times of discharge in both polarities on the centre of screen with the case and Touch Panel terminal grounded.	0/3
	Vibration test	Total amplitude 1.5 mm, f= 10~55 Hz, X,Y,Z directions for each 2 hours.	0/3
	Impact test	Use original jig and make an impact with peak acceleration of 1000 m/s²for 6 ms with half sine-curve at 3 times to each X, Y, Z directions in conformance with JIS 60068-2-27-1995	0/3
Packing Test	Packing Vibration-Proof Test	Acceleration of 19.6 m/s ² with frequency of 10 → 55→ 10 Hz, X, Y, Z direction for each 30 minutes.	0/1 Packing
	Packing Drop Test	Drop from 75 cm high. 1 time to each 6 surfaces, 3 edges, 1 corner	0/1 Packing

Note: Ta=ambient temperature Tp= Panel temperature



Reliability Criteria: measure following parameters after leaving the TFT at 25°C for 2 hours or more.

Item	Standard	Remark
Display quality	No visible abnormalities shall be seen	As per Quality Assurance Specification
Contrast ratio	40 or more	Backlight ON

8 HANDLING PRECAUTIONS

Safety
If the LCD panel breaks, be careful not to get the liquid crystal fluid in your mouth or in your eyes.
If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
When assembling with a zebra connector, clean the surface of the pads with alcohol and keep the surrounding air very clean.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during LCD cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to VDD or VSS.
Do not input any signals before power is turned on. Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use LCD elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life. Direct current causes an electrochemical reaction with remarkable deterioration of the display quality. Give careful consideration to prevent direct current during ON/OFF timing and during operation. Response time is extremely delayed at temperatures lower than the operating temperature range while, at high temperatures, displays become dark. However, this phenomenon is reversible and does not mean a malfunction or a display that has been permanently damaged. If the display area is pushed on hard during operation, some graphics will be abnormally displayed but returns to a normal condition after turning off the display once. Even a small amount of condensation on the contact pads (terminals) can cause an electro-chemical reaction which causes missing rows and columns. Give careful attention to avoid condensation.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).