

# OLED DISPLAY MODULE

## Product Specification

|                          |                      |             |
|--------------------------|----------------------|-------------|
| <b>CUSTOMER</b>          | <b>Standard</b>      |             |
| <b>PRODUCT NUMBER</b>    | <b>DD-12864WO-4A</b> |             |
| <b>CUSTOMER APPROVAL</b> |                      | <b>Date</b> |

| INTERNAL APPROVALS      |                            |                    |
|-------------------------|----------------------------|--------------------|
| Product Mgr             | Doc. Control               | Electr. Eng        |
| <b>Bazile<br/>Peter</b> | <b>Anthony<br/>Perkins</b> | <b>Luo<br/>Luo</b> |
| Date: 10/05/12          | Date: 10/05/12             | Date: 10/05/12     |

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REVISION RECORD



| Rev. | Date      | Page | Chapt. | Comment                            | ECR no. |
|------|-----------|------|--------|------------------------------------|---------|
| A    | 10 May 12 |      |        | First Issue                        |         |
| B    | 28 Nov 12 | 35   | 10     | Update the part number information |         |
|      |           |      |        |                                    |         |
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# 1 MAIN FEATURES

| ITEM                      | CONTENTS                |
|---------------------------|-------------------------|
| Display Format            | 128 x 64 Dots           |
| Overall Dimensions(W*H*T) | 42.04 × 27.22 × 1.45 mm |
| Active Area(W*H)          | 35.052 × 17.516 mm      |
| Viewing Area(W*H)         | 37.052 x 19.516 mm      |
| Display Mode              | Passive Matrix (1.54")  |
| Display Colour            | Monochrome White Colour |
| Driving Method            | 1 / 64 duty             |
| Driver IC                 | SSD1309                 |
| Operating temperature     | -40°C ~ +70°C           |
| Storage temperature       | -40°C ~ +85°C           |

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## 2 MECHANICAL SPECIFICATION

### 2.1 MECHANICAL CHARACTERISTICS

---

| ITEM                 | CHARACTERISTIC       | UNIT |
|----------------------|----------------------|------|
| Display Format       | 128 x 64             | Dots |
| Overall Dimensions   | 42.04 × 27.22 × 1.45 | mm   |
| Viewing Area         | 37.052 x 19.516      | mm   |
| Active Area          | 35.052 × 17.516      | mm   |
| Dot Size             | 0.254 × 0.254        | mm   |
| Dot Pitch            | 0.274 × 0.274        | mm   |
| Weight               | 3.28                 | g    |
| IC Controller/Driver | SSD1309              |      |

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# 2.2 MECHANICAL DRAWING

|           |                  |                            |
|-----------|------------------|----------------------------|
| Item<br>A | Date<br>20111026 | Remark<br>Original Drawing |
|-----------|------------------|----------------------------|

| Pin | Symbol    |
|-----|-----------|
| 1   | VCC (GND) |
| 2   | VSS       |
| 3   | VSS       |
| 4   | VDD       |
| 5   | VDD       |
| 6   | BSI       |
| 7   | CSA       |
| 8   | RESA      |
| 9   | RESA      |
| 10  | DCA       |
| 11  | EDDA      |
| 12  | EDDA      |
| 13  | D0        |
| 14  | D1        |
| 15  | D2        |
| 16  | D3        |
| 17  | D4        |
| 18  | D5        |
| 19  | D6        |
| 20  | D7        |
| 21  | VDD0      |
| 22  | VDD0      |
| 23  | VCC       |
| 24  | VCC (GND) |

**Notes:**

- Color: White
- Driver IC: SSD1309
- FPC Number: UT-0205-P05
- Interface: 8-bit 68XX/60XX Parallel, 4-wire SPI, I2C
- General Tolerance: ±0.30
- The total thickness (1.55 Max) is without polarizer protective film & remove tape. The actual assembled total thickness with above materials should be 1.80 Max.

|                                |                           |  |
|--------------------------------|---------------------------|--|
| Customer Approval<br>Signature | <b>DENSITRON DISPLAYS</b> | DD-12864WO-4A Folding Type OEL Display Module<br>Pixel Number: 128 x 64, Monochrome, COG Package |
| Unit<br>mm                     | Title                     | Material   |
| Tolerance<br>Dimension ±0.3    | By<br>Dora Yang           | Soda Lime / Polyimide  |
| Angle ±1                       | Date<br>20111026          | Scale<br>1:1   |
| General Roughness              | Drawn<br>Ting-Kuo Hu      | Sheet<br>1 of 1  |
| E.E.                           | Panel / E.                | Size<br>A3   |
| Ivy Lo                         | Tiffany Hsu               | Date<br>20111026   |
| P.M.                           | 20111026                  | Pixel Number: 128 x 64, Monochrome, COG Package  |

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### 3 ELECTRICAL SPECIFICATION

#### 3.1 ABSOLUTE MAXIMUM RATINGS

| Item                               | Symbol          | Min    | Max | Unit | Note      |
|------------------------------------|-----------------|--------|-----|------|-----------|
| Supply Voltage for Logic           | V <sub>DD</sub> | -0.3   | 4   | V    | Note 1, 2 |
| Supply Voltage for Display         | V <sub>CC</sub> | 0      | 15  | V    | Note 1, 2 |
| Operating Temperature              | Top             | -40    | 70  | °C   | Note 3    |
| Storage Temperature                | Tstg            | -40    | 85  | °C   | Note 3    |
| Life Time (120 cd/m <sup>2</sup> ) |                 | 10,000 | -   | hour | Note 4    |
| Life Time (80 cd/m <sup>2</sup> )  |                 | 30,000 | -   | hour | Note 4    |
| Life Time (60 cd/m <sup>2</sup> )  |                 | 50,000 | -   | hour | Note 4    |

Note 1: All the above voltages are on the basis of “VSS=0V”.

Note 2: When this module is used beyond above absolute maximum ratings, permanent damage to the module may occur. Also for normal operations it’s desirable to use this module under the conditions according to Section 3.2 “Electrical Characteristics” and section 4 .1 “optical characteristic”. If this module is used beyond these conditions the module may malfunction and the reliability could deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: VCC=12.5V, Ta=25°C, 50% checkerboard.

Software configuration follows Section 5.4 Actual Application Example.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions

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### 3.2 ELECTRICAL CHARACTERISTICS

| Characteristics            | Symbol     | Conditions        | Min     | Typ  | Max     | Unit |
|----------------------------|------------|-------------------|---------|------|---------|------|
| Supply Voltage for Logic   | VDD        | Ta = 25°C         | 1.65    | 2.8  | 3.3     | V    |
| Supply Voltage for Display | VCC        | Ta = 25°C Note 4  | 12      | 12.5 | 13.0    | V    |
| High Level Input           | VIH        | Iout=100μA,3.3MHz | 0.8xVDD | -    | VDD     | V    |
| Low Level Input            | VIL        | Iout=100μA,3.3MHz | 0       | -    | 0.2xVDD | V    |
| High Level Output          | VOH        | Iout=100μA,3.3MHz | 0.9xVDD | -    | VDD     | V    |
| Low Level Output           | VOL        | Iout=100μA,3.3MHz | 0       | -    | 0.1xVDD | V    |
| Operating Current for VDD  | IDD        |                   |         | 180  | 300     | μA   |
| Operating Current for VCC  | ICC        | Note 1            |         | 12.7 | 15.9    | mA   |
|                            |            | Note 2            |         | 20.5 | 25.6    | mA   |
|                            |            | Note 3            |         | 35.8 | 44.8    | mA   |
| Sleep Mode Current for VDD | IDD, SLEEP |                   |         | 1    | 5       | μA   |
| Sleep Mode Current for VCC | ICC, SLEEP |                   |         | 2    | 10      | μA   |

Note 1 V<sub>DD</sub> = 2.8V, V<sub>CC</sub> = 12.5V, 30% Display area turned on

Note 2 V<sub>DD</sub> = 2.8V, V<sub>CC</sub> = 12.5V, 50% Display area turned on.

Note 3 V<sub>DD</sub> = 2.8V, V<sub>CC</sub> = 12.5V, 100% Display area turned on

Note 4 Brightness (L<sub>br</sub>) and Supply Voltage for Display (V<sub>CC</sub>) are subject to the change of the panel characteristics.

\* Software configuration follows Section 5.4 Actual Application Example.

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### 3.3 INTERFACE PIN ASSIGNMENT

| No.           | Symbol     | I/O | Function  |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
|---------------|------------|-----|---|-----|-----|-----|-----|---|---|------------|---|---|---------------|---|---|---------------|---|---|
| 1             | N.C. (GND) | -   | <b>Reserved Pin (Supporting Pin)</b><br>The supporting pin can reduce the influences from stresses on the function pins. This pin must be connected to external ground as the ESD protection circuit.   |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 2             | VLSS       | P   | <b>Ground of Analogue Circuit</b><br>This is an analogue ground pin. It should be connected to VSS externally.  |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 3             | VSS        | P   | <b>Ground of Logic Circuit</b><br>This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.   |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 4             | N.C        | -   | <b>Reserved Pin</b><br>The N.C. pins between function pins are reserved for compatible and flexible design.   |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 5             | VDD        | P   | <b>Power Supply for Logic Circuit</b><br>This is a voltage supply pin. It must be connected to external source  |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 6             | BS1        | I   | <b>Communicating Protocol Select</b><br>These pins are MCU interface selection input. See the following table: <table border="1" data-bbox="699 1288 1286 1480"> <thead> <tr> <th></th> <th>BS1</th> <th>BS2</th> </tr> </thead> <tbody> <tr> <td>I2C</td> <td>1</td> <td>0</td> </tr> <tr> <td>4-wire SPI</td> <td>0</td> <td>0</td> </tr> <tr> <td>68XX-parallel</td> <td>0</td> <td>1</td> </tr> <tr> <td>80XX-parallel</td> <td>1</td> <td>1</td> </tr> </tbody> </table> |     | BS1 | BS2 | I2C | 1 | 0 | 4-wire SPI | 0 | 0 | 68XX-parallel | 0 | 1 | 80XX-parallel | 1 | 1 |
|               | BS1        |     |   | BS2 |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| I2C           | 1          |     |   | 0   |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 4-wire SPI    | 0          |     |   | 0   |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 68XX-parallel | 0          | 1   |   |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 80XX-parallel | 1          | 1   |   |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 7             | BS2        |     |   |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 8             | CS#        | I   | <b>Chip Select</b><br>This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.   |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |
| 9             | RES#       | I   | <b>Power Reset for Controller and Driver</b><br>This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation  |     |     |     |     |   |   |            |   |   |               |   |   |               |   |   |

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|       |       |     |  |
|-------|-------|-----|--|
| 10    | D/C#  | I   | <p><b>Data/Command Control</b></p> <p>This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.</p> <p>When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.</p> <p>For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</p> |
| 11    | R/W#  | I   | <p><b>Read/Write Select or Write</b></p> <p>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it to “Low” for write mode.</p> <p>When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS</p>   |
| 12    | E/RD# | I   | <p><b>Read/Write Enable or Read</b></p> <p>This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to VSS</p>   |
| 13~20 | D0~D7 | I/O | <p><b>Host Data Input/output Bus</b></p> <p>These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2C mode is selected, D2 &amp; D1 should be tied together and serve as SDAout &amp; SDAin in application and D0 is the serial clock input SCL.</p> <p>Unused pins must be connected to VSS except for D2 in serial mode</p>  |
| 21    | IREF  | I   | <p><b>Current Reference for Brightness Adjustment</b></p> <p>This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 10μA maximum..</p>   |

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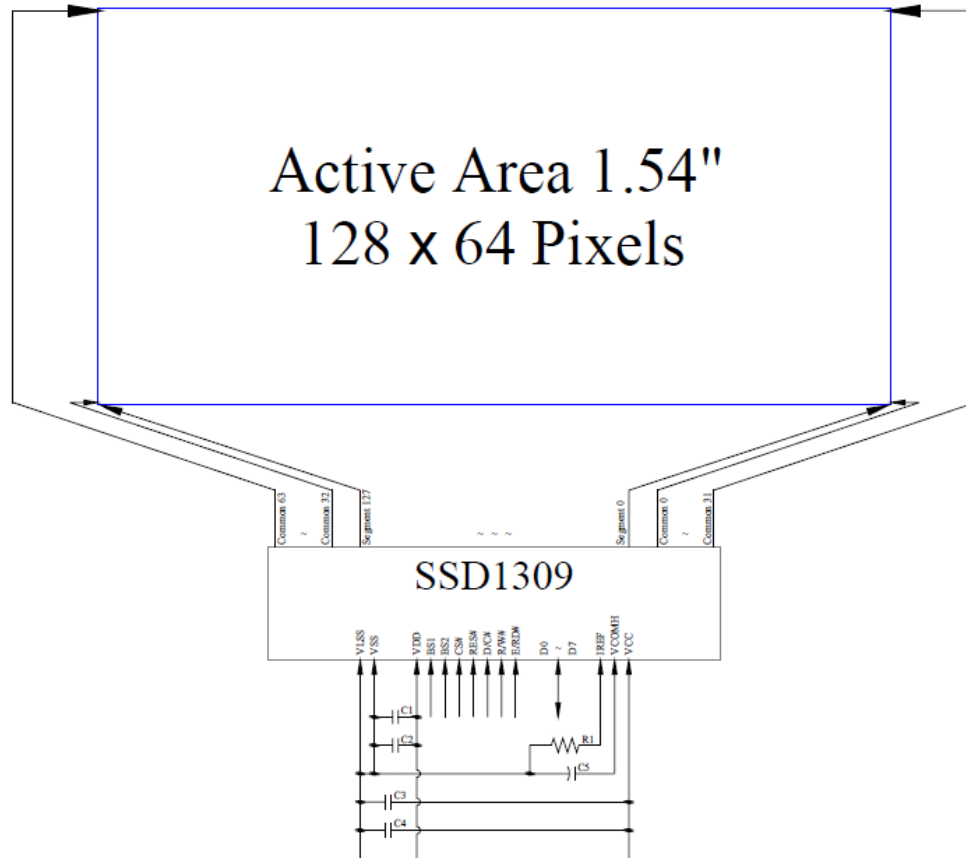
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|    |            |   |  |
|----|------------|---|--|
| 22 | VCOMH      | O | <p><b>Voltage Output High Level for COM Signal</b></p> <p>This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</p>             |
| 23 | VCC        | P | <p><b>Power Supply for OEL Panel</b></p> <p>This is the most positive voltage supply pin of the chip. It must be supplied externally.</p>  |
| 24 | N.C. (GND) | - | <p><b>Reserved Pin (Supporting Pin)</b></p> <p>The supporting pin can reduce the influences from stresses on the function pins. This pin must be connected to external ground as the ESD protection circuit.</p> |

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### 3.4 BLOCK DIAGRAM



MCU Interface Selection:           BS1 and BS2  
 Pins connected to MCU interface: CS#, RES#, D/C#, R/W#, E/RD#, and D0~D7

- C1, C3: 0.1µF
- C2:    4.7µF
- C4:    10µF
- C5:    4.7µF / 25V Tantalum Capacitor
- R1:    910kΩ,  $R1 = (\text{Voltage at IREF} - \text{BGGND}) / \text{IREF}$

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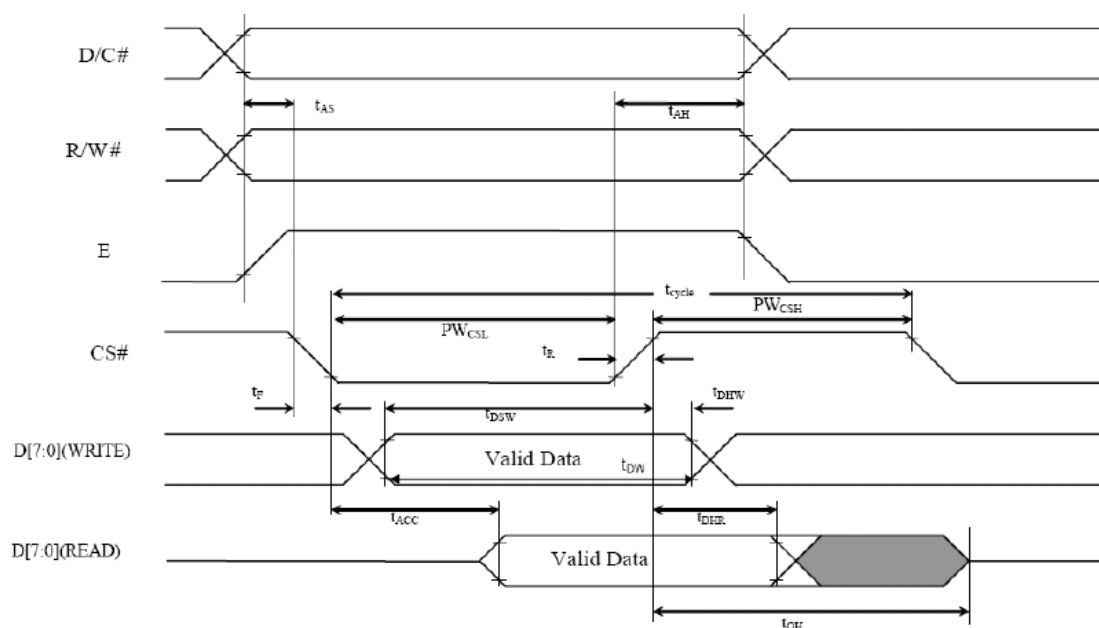
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### 3.5 AC CHARACTERISTICS

#### 3.5.1 68XX-Series MPU Parallel Interface Timing Characteristics

| Characteristics   | Symbol      | Min       | Max | Unit |
|---|-------------|-----------|-----|------|
| Clock Cycle Time  | $t_{cycle}$ | 300       | -   | ns   |
| Address Setup Time  | $t_{AS}$    | 20        | -   | ns   |
| Address Hold Time   | $t_{AH}$    | 0         | -   | ns   |
| Data Write Time   | $t_{DW}$    | 80        | -   | ns   |
| Write Data Setup Time   | $t_{DSW}$   | 40        | -   | ns   |
| Write Data Hold Time  | $t_{DHW}$   | 20        | -   | ns   |
| Read Data Hold Time   | $t_{DHR}$   | 20        | -   | ns   |
| Output Disable Time   | $t_{OH}$    | -         | 70  | ns   |
| Access Time   | $t_{ACC}$   | -         | 140 | ns   |
| Chip Select Low Pulse Width (Read)<br>Chip Select Low Pulse Width (Write)   | $PW_{CSL}$  | 120<br>60 | -   | ns   |
| Chip Select High Pulse Width (Read)<br>Chip Select High Pulse Width (Write) | $PW_{CSH}$  | 60<br>60  | -   | ns   |
| Rise Time   | $t_R$       | -         | 40  | ns   |
| Fall Time   | $t_F$       | -         | 40  | ns   |

( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_a = 25^\circ C$ )



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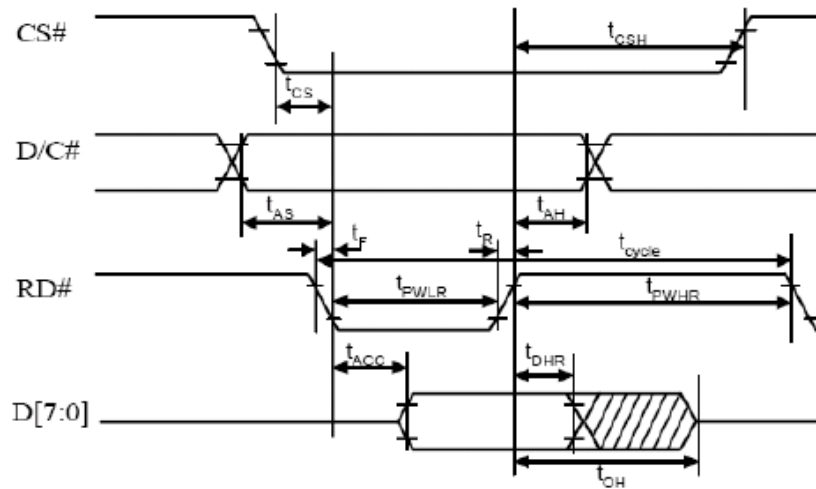
### 3.5.2 8080-Series MPU Parallel Interface Timing Characteristics

| Characteristics                      | Symbol      | Min | Max | Unit |
|--------------------------------------|-------------|-----|-----|------|
| Clock Cycle Time                     | $t_{cycle}$ | 300 | -   | ns   |
| Address Setup Time                   | $t_{AS}$    | 20  | -   | ns   |
| Address Hold Time                    | $t_{AH}$    | 0   | -   | ns   |
| Data Write Time                      | $t_{DW}$    | 70  |     | ns   |
| Write Data Setup Time                | $t_{DSW}$   | 40  | -   | ns   |
| Write Data Hold Time                 | $t_{DHW}$   | 15  | -   | ns   |
| Read Data Hold Time                  | $t_{DHR}$   | 20  | -   | ns   |
| Output Disable Time                  | $t_{OH}$    | -   | 70  | ns   |
| Access Time                          | $t_{ACC}$   | -   | 140 | ns   |
| Read Low Time                        | $t_{PWLR}$  | 120 | -   | ns   |
| Write Low Time                       | $t_{PWLW}$  | 60  | -   | ns   |
| Read High Time                       | $t_{PWHR}$  | 60  | -   | ns   |
| Write High Time                      | $t_{PWHW}$  | 60  | -   | ns   |
| Chip Select Setup Time               | $t_{CS}$    | 0   | -   | ns   |
| Chip Select Hold Time to Read Signal | $t_{CSH}$   | 0   | -   | ns   |
| Chip Select Hold Time                | $t_{CSF}$   | 20  | -   | ns   |
| Rise Time                            | $t_R$       | -   | 40  | ns   |
| Fall Time                            | $t_F$       | -   | 40  | ns   |

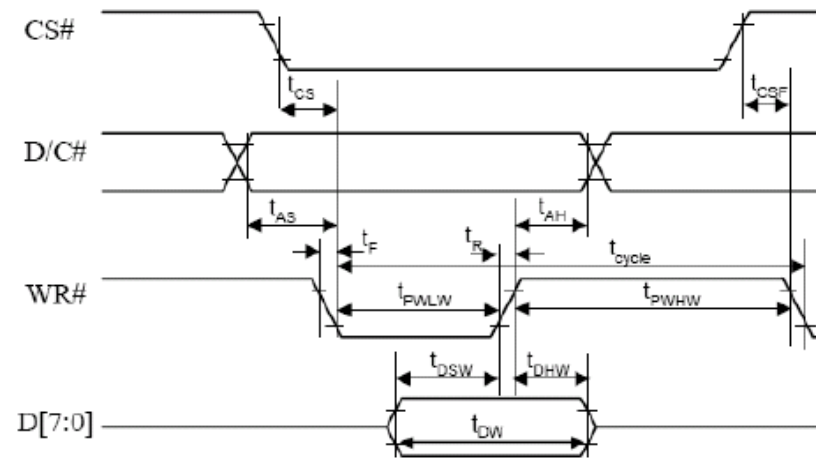
( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_a = 25^\circ C$ )

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**( Read Timing )**



**( Write Timing )**

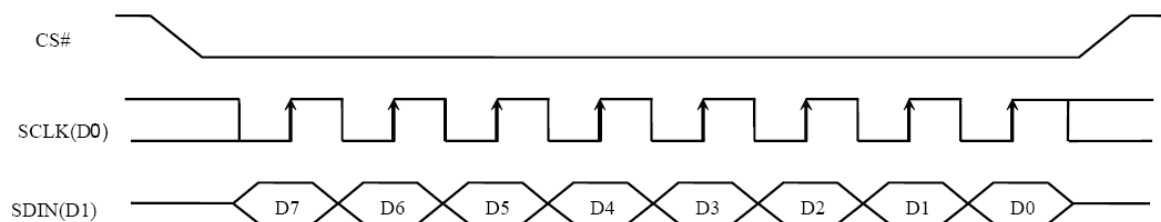
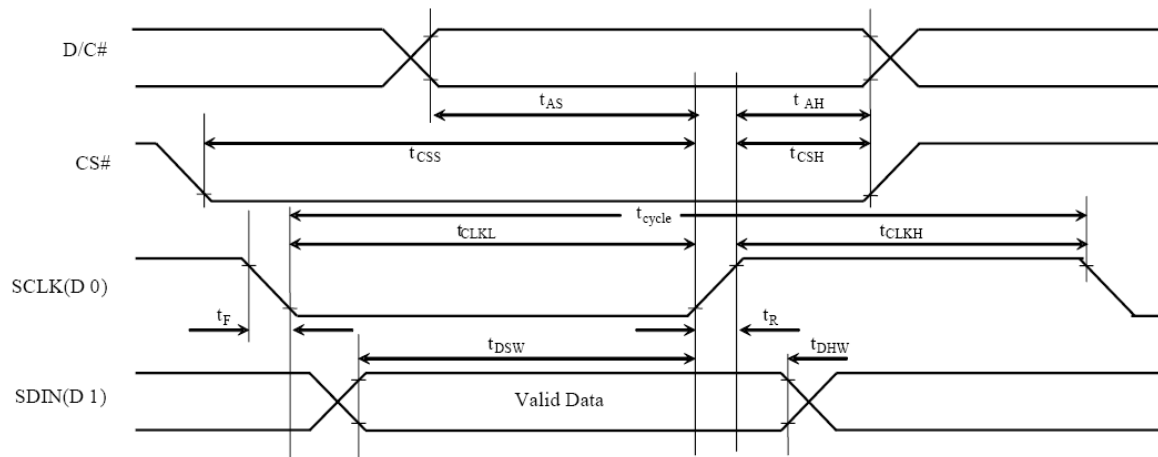
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### 3.5.3 Serial Interface Timing Characteristics (4-wire SPI)

| Characteristics        | Symbol      | Min | Max | Unit |
|------------------------|-------------|-----|-----|------|
| Clock Cycle Time       | $t_{cycle}$ | 100 | -   | ns   |
| Address Setup Time     | $t_{AS}$    | 15  | -   | ns   |
| Address Hold Time      | $t_{AH}$    | 15  | -   | ns   |
| Chip Select Setup Time | $t_{CSS}$   | 20  | -   | ns   |
| Chip Select Hold Time  | $t_{CSH}$   | 50  | -   | ns   |
| Data write Time        | $t_{DW}$    | 55  | -   | ns   |
| Write Data Setup Time  | $t_{DSW}$   | 15  | -   | Ns   |
| Write Data Hold Time   | $t_{DHW}$   | 15  | -   | Ns   |
| Clock Low Time         | $t_{CLKL}$  | 50  | -   | Ns   |
| Clock High Time        | $t_{CLKH}$  | 50  | -   | Ns   |
| Rise Time              | $t_R$       | -   | 40  | Ns   |
| Fall Time              | $t_F$       | -   | 40  | Ns   |

( $V_{DD} - V_{SS} = 1.65V$  to  $3.3V$ ,  $T_a = 25^\circ C$ )

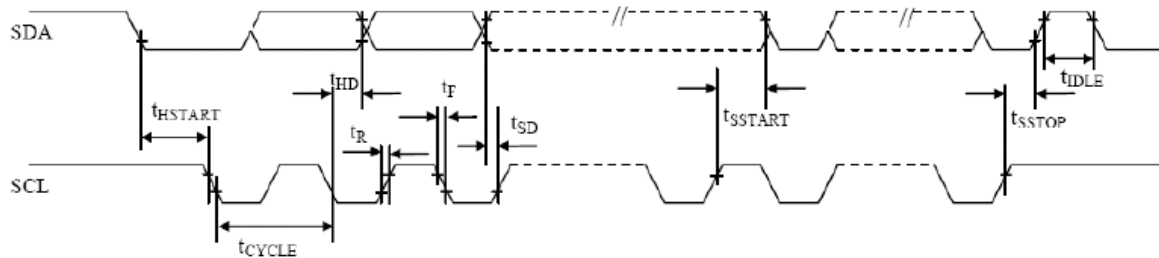




### 3.5.4 I2C Interface Timing Characteristics:

| Symbol              | Description  | Min | Max | Unit |
|---------------------|--|-----|-----|------|
| $t_{\text{cycle}}$  | Clock Cycle Time   | 2.5 | -   | us   |
| $t_{\text{HSTART}}$ | Start Condition Hold Time  | 0.6 | -   | us   |
| $t_{\text{HD}}$     | Data Hold Time (for “SDA <sub>OUT</sub> ” Pin)                               | 0   | -   | ns   |
|                     | Data Hold Time (for “SDA <sub>IN</sub> ” Pin)                                | 300 |     |      |
| $t_{\text{SD}}$     | Data Setup Time  | 100 | -   | ns   |
| $t_{\text{SSTART}}$ | Start Condition Setup Time<br>(Only relevant for a repeated Start condition) | 0.6 | -   | us   |
| $t_{\text{SSTOP}}$  | Stop Condition Setup Time  | 0.6 | -   | us   |
| $t_{\text{R}}$      | Rise Time for Data and Clock Pin   |     | 300 | ns   |
| $t_{\text{F}}$      | Fall Time for Data and Clock Pin   |     | 300 | ns   |
| $t_{\text{IDLE}}$   | Idle Time before a New Transmission can Start                                | 1.3 | -   | us   |

\* ( $V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$ ,  $T_{\text{a}} = 25^{\circ}\text{C}$ )



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## 4 OPTICAL SPECIFICATION

### 4.1 OPTICAL CHARACTERISTICS

| Characteristics    | Symbol   | Condition   | Min  | Typ       | Max  | Unit              |
|--------------------|----------|-------------|------|-----------|------|-------------------|
| Brightness         | $L_{br}$ | Note 1      | 100  | 120       | -    | cd/m <sup>2</sup> |
| C.I.E.(White)      | (X)      | C.I.E. 1931 | 0.25 | 0.29      | 0.33 | -                 |
|                    | (Y)      |             | 0.27 | 0.31      | 0.35 |                   |
| Dark Room Contrast | CR       |             | -    | >10,000:1 | -    | -                 |
| Viewing Angle      |          |             | -    | Free      | -    | degree            |

Note 1 Brightness ( $L_{br}$ ) and Supply Voltage for Display ( $V_{CC}$ ) are subject to the change of the panel characteristics.

\* Software configuration follows Section 5.4 Actual Application example.

\* Optical measurement taken at  $V_{DD} = 2.8V$ ,  $V_{CC} = 12.5V$

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## 5 FUNCTIONAL SPECIFICATION

### 5.1 COMMANDS

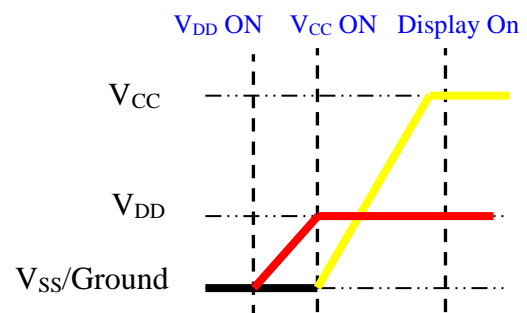
Please refer to the Technical Manual for the SSD1309

### 5.2 POWER UP/DOWN SEQUENCE

To protect the panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the panel enough time to complete the action of charge and discharge before/after the operation.

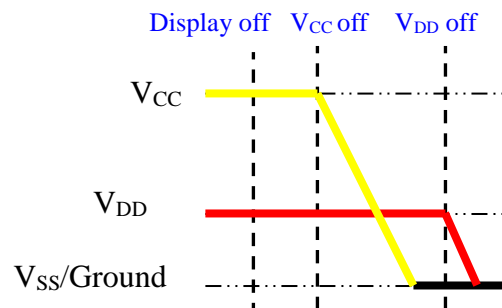
#### 5.2.1 POWER UP SEQUENCE

1. Power up  $V_{DD}$
2. Send Display off command
3. Initialization 4. Clear Screen
5. Power up  $V_{CC}$
6. Delay 100ms  
(When  $V_{CC}$  is stable)
7. Send Display on command



#### 5.2.2 POWER DOWN SEQUENCE

1. Send Display off command
2. Power down  $V_{CC}$
3. Delay 100ms  
(When  $V_{CC}$  is reach 0 and panel is completely discharges)
4. Power down  $V_{DD}$



Note:

- 1) Since an ESD protection circuit is connected between  $V_{DD}$  and  $V_{CC}$  inside the driver IC,  $V_{CC}$  becomes lower than  $V_{DD}$  whenever  $V_{DD}$  is ON and  $V_{CC}$  is OFF.
- 2)  $V_{CC}$  should be kept float (disable) when it is OFF.
- 3) Power Pins ( $V_{DD}$ ,  $V_{CC}$ ) can never be pulled to ground under any circumstance.
- 4)  $V_{DD}$  should not be power down before  $V_{CC}$  power down.

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### 5.3 RESET CIRCUIT

---

When RES# input is low, the chip is initialized with the following status:

1. Display is off
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

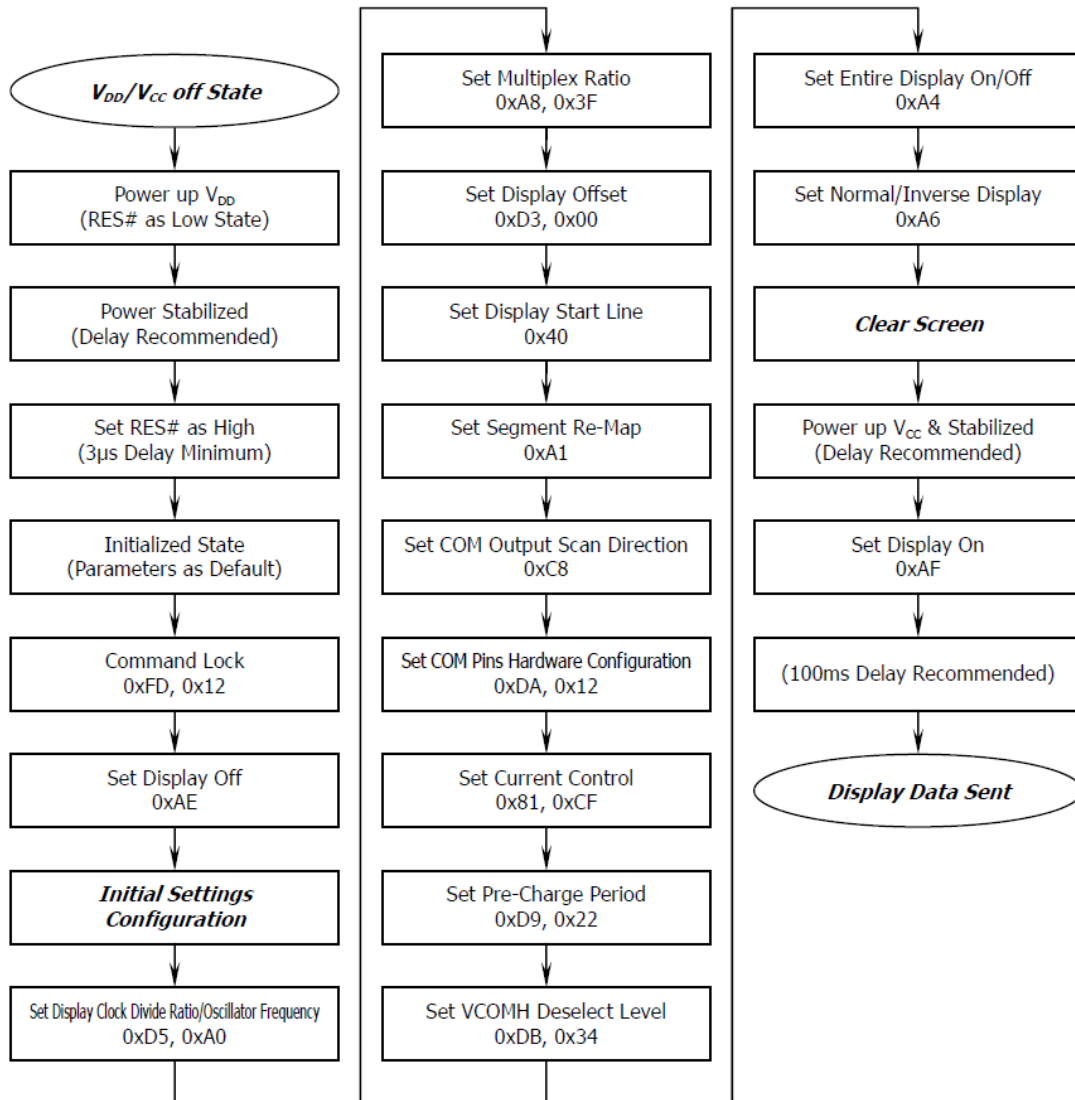
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## 5.4 ACTUAL APPLICATION EXAMPLE

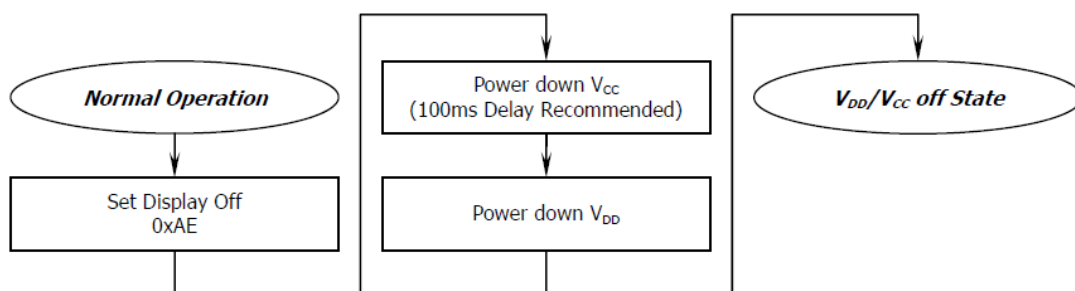
Command usage and explanation of an actual example

<Power up Sequence>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

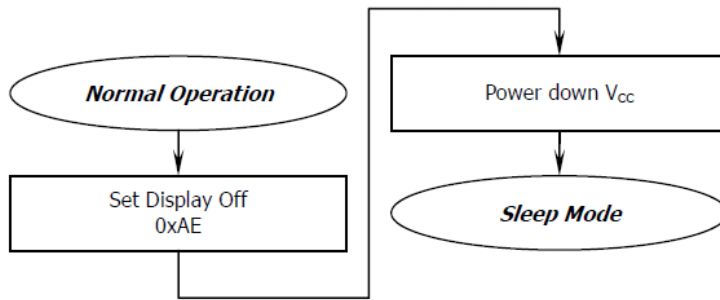
<Power down Sequence>



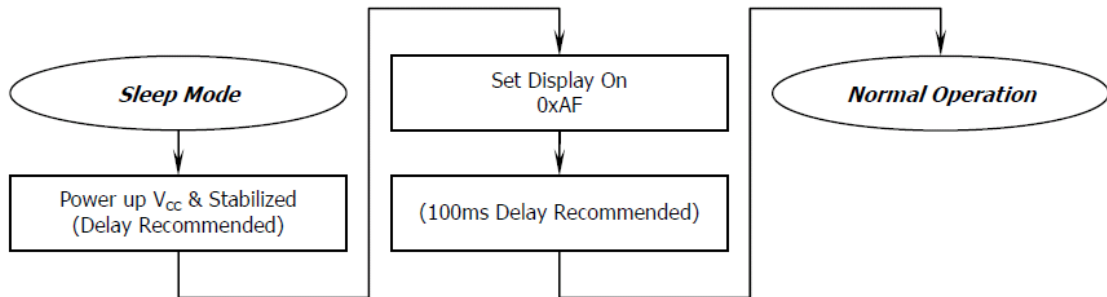
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<Entering Sleep Mode>



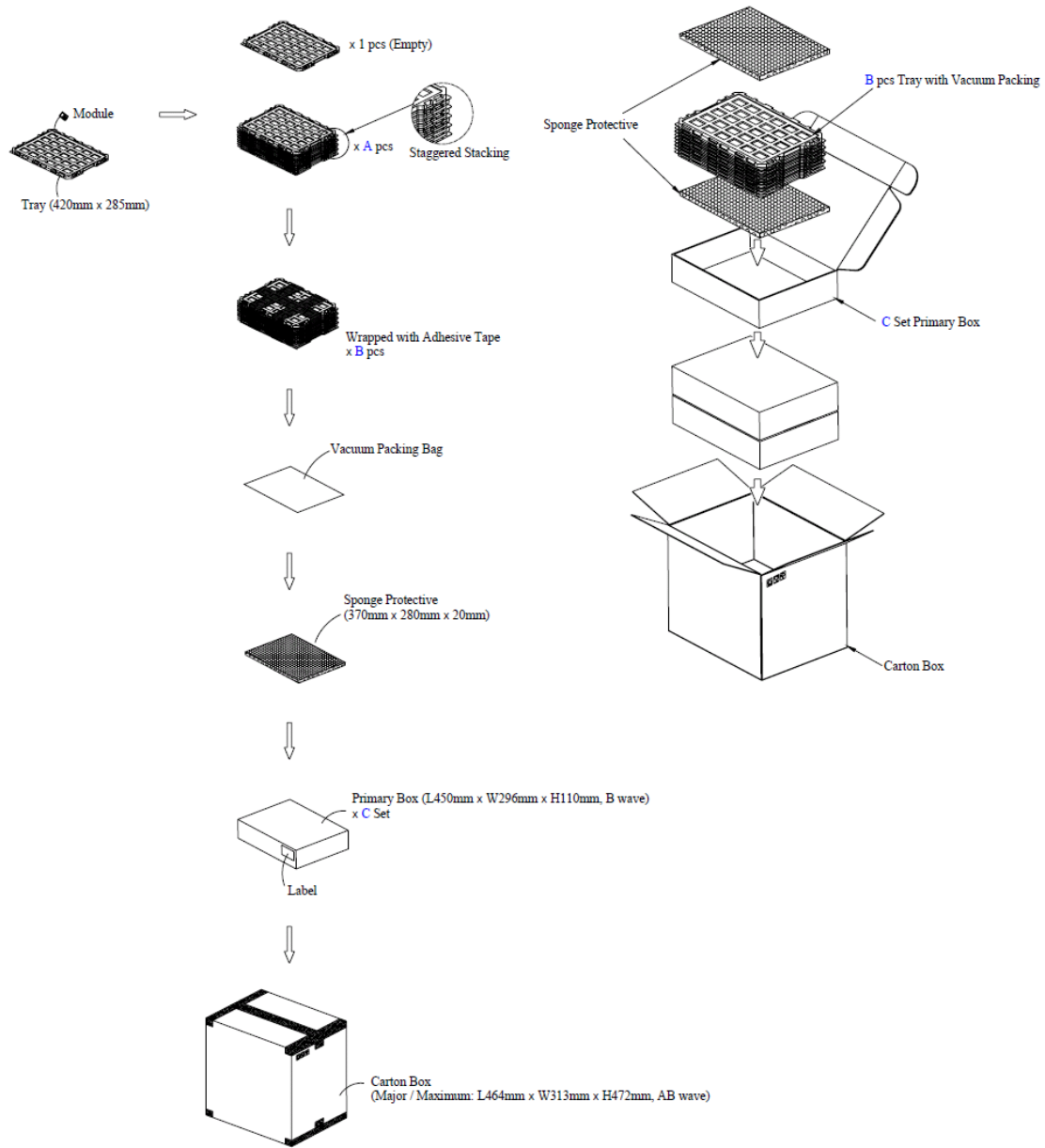
<Exiting Sleep Mode>



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## 6 PACKAGING AND LABELLING SPECIFICATION



| Item                     | Quantity   |   |
|--------------------------|------------|---|
| <b>Module</b>            | <b>270</b> | <b>per Primary Box</b>                          |
| <b>Holding Trays</b> (A) | <b>15</b>  | <b>per Primary Box</b>                          |
| <b>Total Trays</b> (B)   | <b>16</b>  | <b>per Primary Box (Including 1 Empty Tray)</b> |
| <b>Primary Box</b> (C)   | <b>1~4</b> | <b>per Carton (4 as Major / Maximum)</b>        |

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## 6.1 LABELLING & MARKING

|  |
|--|
| DENSITRON<br>DD-12864WO-4A<br>TW YY MM |
|--|

## 7 QUALITY ASSURANCE SPECIFICATION

### 7.1 CONFORMITY

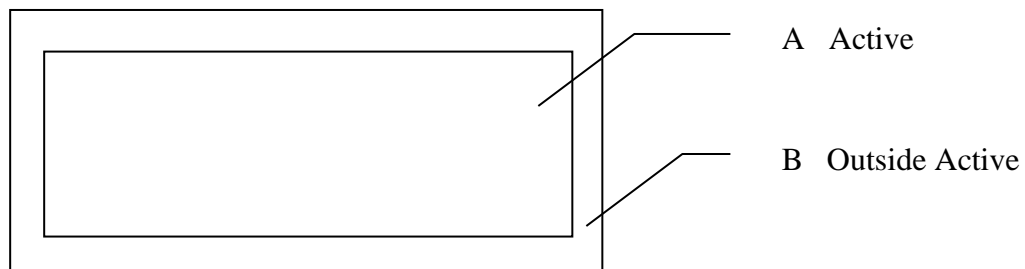
The performance, function and reliability of the shipped products conform to the Product Specification.

### 7.2 DELIVERY ASSURANCE

#### 7.2.1 DELIVERY INSPECTION STANDARDS

Level II, normal inspection, single sampling, MIL-STD-105E

#### 7.2.2 Zone definition



#### 7.2.3 Visual inspection

Test and measurement to be conducted under following conditions:

|   |          |
|---|----------|
| Temperature:  | 23±5°C   |
| Humidity:   | 55±15%RH |
| Fluorescent lamp:   | 30 W     |
| Distance between the Panel & Eyes of the Inspector:           | ≥30cm    |
| Distance between the Panel & the lamp:                        | ≥50cm    |
| Finger glove (or finger cover) must be worn by the inspector. |          |
| Inspection table or jig must be anti-electrostatic            |          |

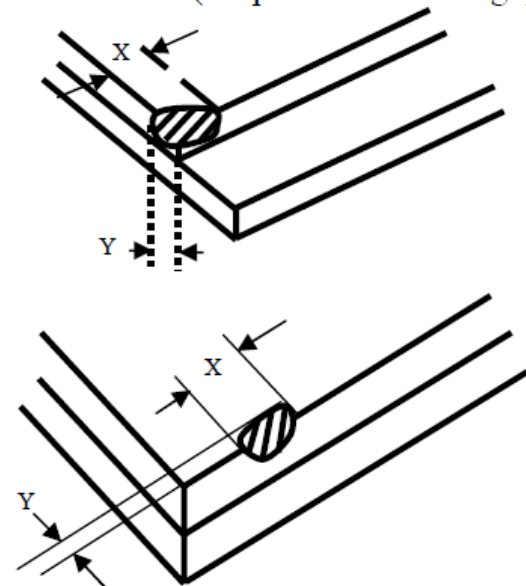
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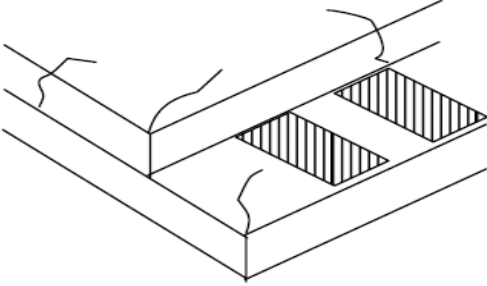

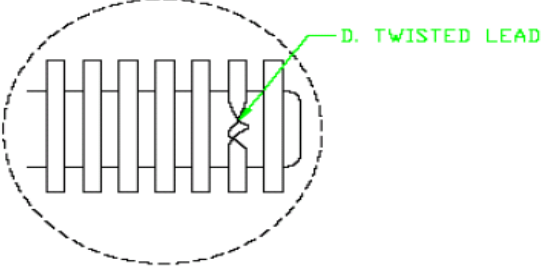
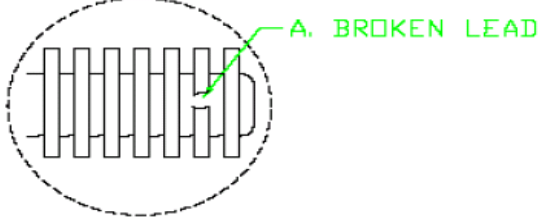
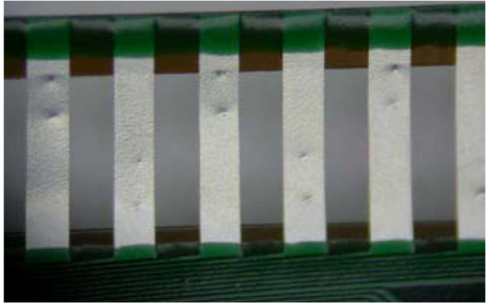
### 7.2.4 Standard of appearance inspection

| Partition | AQL  | Definition                              |
|-----------|------|---|
| Major     | 0.65 | Defects in Pattern Check (Display On)   |
| Minor     | 1.0  | Defects in Cosmetic Check (Display Off) |

| Check Item                | Classification | Criteria  |
|---------------------------|----------------|---|
| Panel<br>General Chipping | Minor          | <p> <math>X &gt; 6 \text{ mm}</math> (Along with Edge)<br/> <math>Y &gt; 1 \text{ mm}</math> (Perpendicular to edge) </p>  |

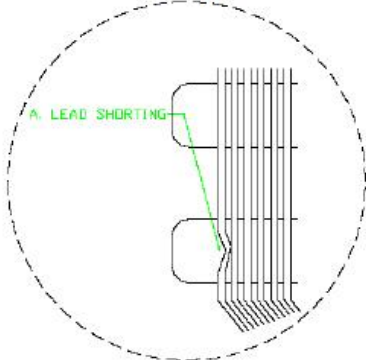
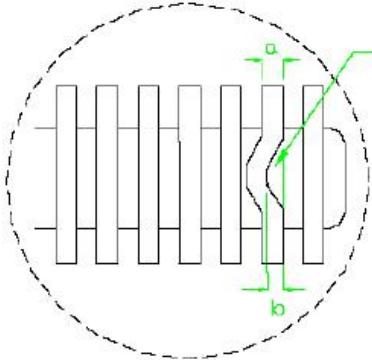
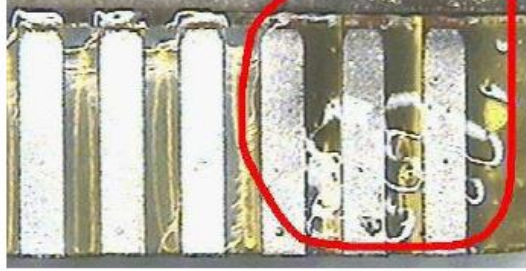
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| Check Item                        | Classification | Criteria   |
|-----------------------------------|----------------|--|
| Panel Crack                       | Minor          | <p>Any crack is not allowable.</p>             |
| Copper Exposed (Even Pin or Film) | Minor          | <p>Not Allowable by Naked Eye Inspection</p>   |
| Film or Trace Damage              | Minor          |    |
| Terminal Lead Twist               | Minor          | <p>Not Allowable</p>  <p>D. TWISTED LEAD</p> |
| Terminal Lead Broken              | Minor          | <p>Not Allowable</p>  <p>A. BROKEN LEAD</p>  |
| Terminal Lead Prober Mark         | Acceptable     |    |

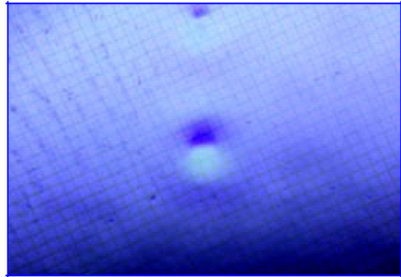
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| Check Item   | Classification | Criteria   |
|--|----------------|--|
| Terminal Lead Bent<br>(Not Twist or Broken)                      | Minor          | NG if any bent lead cause lead shorting.<br>                   |
|  | Minor          | NG for horizontally bent lead more than 50% of its width.<br> |
| Glue or Contamination on Pin<br>(Couldn't Be Removed by Alcohol) | Minor          |    |
| Ink Marking on Back Side of panel<br>(Exclude on Film)           | Acceptable     | Ignore for Any   |

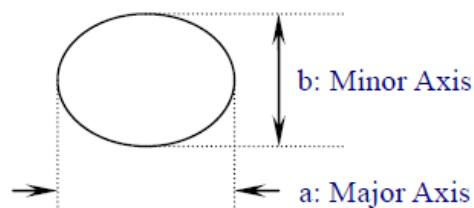
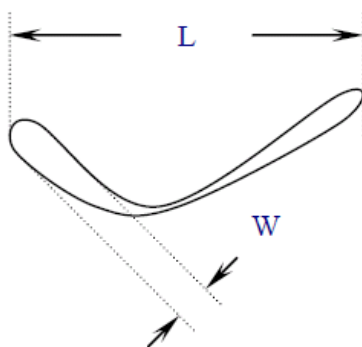
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| Check Item  | Classification | Criteria  |
|---|----------------|---|
| Any Dirt & Scratch on Polarizer's Protective Film             | Acceptable     | Ignore for not Affect the Polarizer   |
| Scratches, Fiber, Line-Shape Defect (On Polarizer)            | Minor          | $W \leq 0.1$ Ignore<br>$W > 0.1, L \leq 2$ $n \leq 1$<br>$L > 2$ $n = 0$  |
| Dirt, Black Spot, Foreign Material, (On Polarizer)            | Minor          | $\Phi \leq 0.1$ Ignore<br>$0.1 < \Phi \leq 0.25$ $n \leq 1$<br>$0.25 < \Phi$ $n = 0$  |
| Dent, Bubbles, White spot (Any Transparent Spot on Polarizer) | Minor          | $\Phi \leq 0.5$<br>→ Ignore if no Influence on Display<br>$0.5 < \Phi$ $n = 0$<br> |
| Fingerprint, Flow Mark (On Polarizer)                         | Minor          | Not Allowable   |

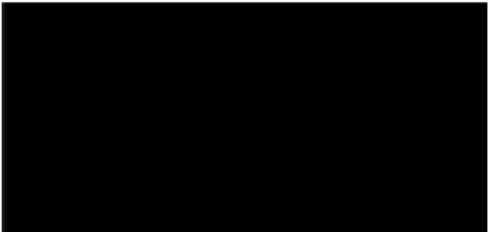
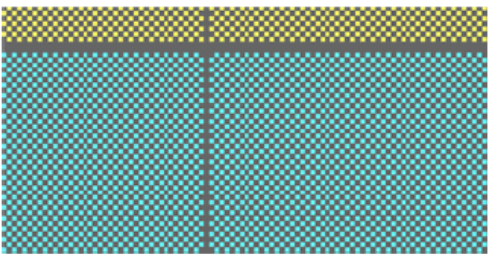
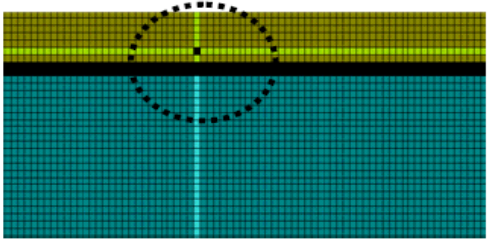
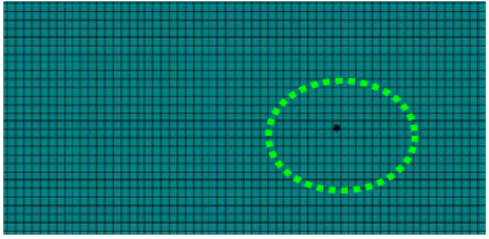
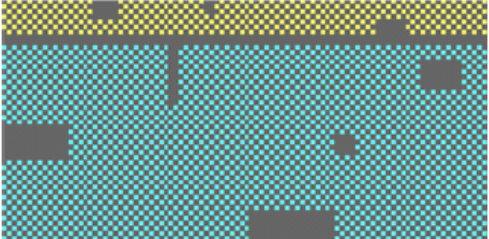
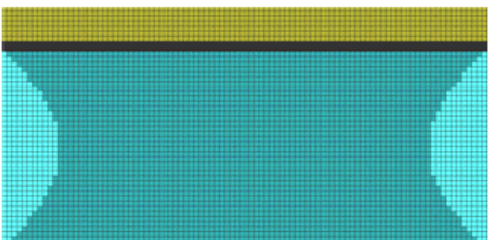
\* Protective film should not be tear off when cosmetic check.

\*\* Definition of W & L &  $\Phi$  (Unit: mm):  $\Phi = (a + b) / 2$



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| Check Item    | Classification | Criteria   |
|---------------|----------------|--|
| No Display    | Major          |    |
| Flicker       | Major          | Not Allowable  |
| Missing Line  | Major          |    |
| Pixel Short   | Major          |   |
| Darker Pixel  | Major          |  |
| Wrong Display | Major          |  |
| Un-uniform    | Major          |  |

## ***7.3 DEALING WITH CUSTOMER COMPLAINTS***

---

### **7.3.1 Non-conforming analysis**

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.

If the analysis cannot be completed on time, Densitron must inform the purchaser.

### **7.3.2 Handling of non-conforming displays**

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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## 8 RELIABILITY SPECIFICATION

### 8.1 RELIABILITY TESTS

| Test Item   | Test Condition   | Evaluation and assessment                   |
|---|--|---|
| High Temperature Operation                          | 70°C, 240 hours  | No abnormalities in function and appearance |
| Low Temperature Operation                           | -40°C, 240 hours   | No abnormalities in function and appearance |
| High Temperature Storage                            | 85°C, 240 hours  | No abnormalities in function and appearance |
| Low Temperature Storage                             | -40°C, 240 hours   | No abnormalities in function and appearance |
| High Temperature & High Humidity Storage(Operation) | 60°C, 90%RH, 120 hours                                     | No abnormalities in function and appearance |
| Thermal Shock                                       | 24 cycle of<br>-40°C 1 Hour,<br>R.T. 5 min,<br>85°C 1 Hour | No abnormalities in function and appearance |

- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

#### 8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5 °C; 55±15% RH

### 8.2 LIFE TIME

| Item                  | Description   |                       |           |                      |           |                      |           |
|-----------------------|---|-----------------------|-----------|----------------------|-----------|----------------------|-----------|
| 1                     | Function, performance, appearance, etc. shall be free from remarkable deterioration more than 15,000 hours at 100cd.m2 under ordinary operating conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight. VCC = 12.0V, Ta = 25°C, 50% Checkerboard.<br>Software configuration follows Section 5.4 Initialization. <table border="1" data-bbox="300 1503 1241 1637"> <tr> <td>Life Time (120 cd/m2)</td> <td>10,000 hr</td> </tr> <tr> <td>Life Time (80 cd/m2)</td> <td>30,000 hr</td> </tr> <tr> <td>Life Time (60 cd/m2)</td> <td>50,000 hr</td> </tr> </table> | Life Time (120 cd/m2) | 10,000 hr | Life Time (80 cd/m2) | 30,000 hr | Life Time (60 cd/m2) | 50,000 hr |
| Life Time (120 cd/m2) | 10,000 hr   |                       |           |                      |           |                      |           |
| Life Time (80 cd/m2)  | 30,000 hr   |                       |           |                      |           |                      |           |
| Life Time (60 cd/m2)  | 50,000 hr   |                       |           |                      |           |                      |           |
| 2                     | End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.   |                       |           |                      |           |                      |           |

### 8.3 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

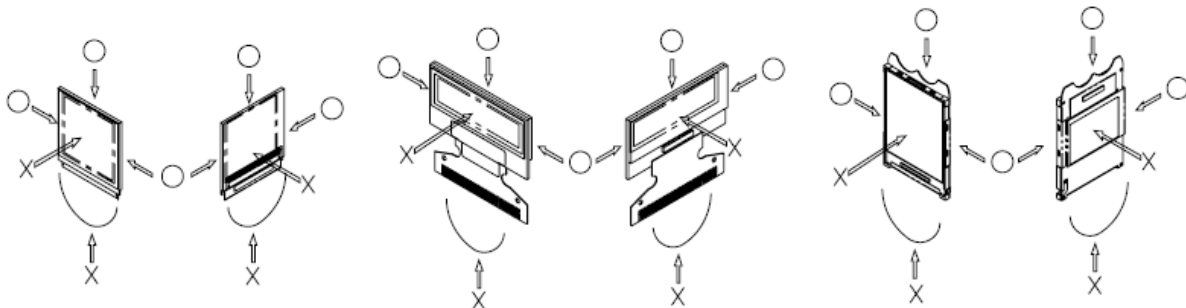
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## 9 HANDLING PRECAUTIONS

### 9.1 HANDLING PRECAUTIONS

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such as dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
- 5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
  - \* Scotch Mending Tape No. 810 or an equivalent
 Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.  
 Also, pay attention that the following liquid and solvent may spoil the polarizer:
  - \* Water
  - \* Ketone
  - \* Aromatic Solvents
- 6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 7) Do not apply stress to the LSI chips and the surrounding molded sections.
- 8) Do not disassemble nor modify the OEL display module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
  - \* Be sure to make human body grounding when handling OEL display modules.
  - \* Be sure to ground tools to use or assembly such as soldering irons.
  - \* To suppress generation of static electricity, avoid carrying out assembly work under dry environments.

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\* Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.

- 11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
- 12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

## 9.2 STORAGE PRECAUTIONS

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- 1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
- 2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

## 9.3 DESIGNING PRECAUTIONS

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- 1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OEL display module, fasten the external plastic housing section.
- 7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066  
\* Connection (contact) to any other potential than the above may lead to rupture of the IC.

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## 9.4 OTHER PRECAUTIONS

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- 1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- 2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
  - \* Pins and electrodes
  - \* Pattern layouts such as the FPC
- 3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
  - \* Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
  - \* Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
- 4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

## 9.5 PRECAUTIONS WHEN DISPOSING OF THE OEL DISPLAY MODULES

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- 1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

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## 10 SUPPORTED ACCESSORIES

### 10.1 DUO KIT

Densitron has developed an easy to use yet powerful development and demonstration tool for driving its range of Passive Matrix OLED displays from the USB port of a PC.

DUO (Densitron USB OLED) kit is hot pluggable and does not require extra cables or power supply to run, allowing users to be up and running in minutes.

The kit consists of an OLED display with transition Board, USB controller card, mini USB cable and a CD with software application and drivers.



**Part number: PDK-N-12864WO-4A**

### 10.2 TRANSITION BOARD CARD

A Transition board card is like a daughterboard which is meant to be a circuit board for connections between the baseboards (DUO).

It has connector pins for interfacing between the display and the baseboards.

It also includes the OLED display.

**Part number: PDT-N-12864WO-4A**

### 10.3 CONNECTOR BOARD CARD

A Connector board is a daughterboard which allows a connection between customer's microprocessor or microcontroller (customer's system) to the display.

**Part number: EVK-CONNECT-015**

### 10.4 CONNECTOR

Type: ZIF connector

| No. of connections | Pitch (mm) | Manufacturer | Manufacturer part no. | Distributor part no.                   |
|--------------------|------------|--------------|-----------------------|--|
| 24                 | 0.50       | Omron        | XF2M-2415-1A          | Farnell/1112559<br>Digikey/ OR721CT-ND |

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